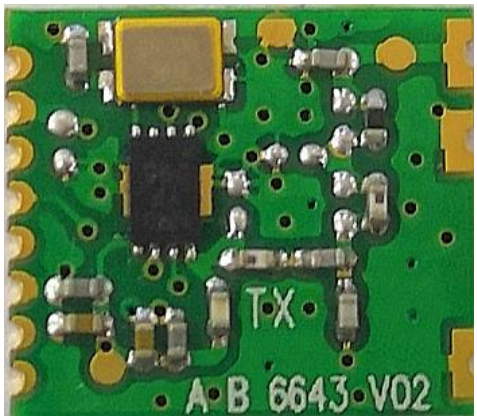
Sub GHz FSK/OOK Transmitter Module DATASHEET

GENERAL DESCRIPTION

The HC1243 is an ultra-low-cost, fully integrated FSK or OOK transmitter suitable for operation between 310 and 450 MHz, 860 and 870 MHz, as well as 902 and 928 MHz.

For applications where economy is paramount, the HC1243 may be used without the requirement for configuration via an MCU. However, in conjunction with a microcontroller the communication link parameters may be re-configured. Including, output power, modulation format and operating channel.

The HC1243 offers integrated radio performance with cost efficiency and is suited for operation in North America FCC Part 15.231, FCC Part 15.247 FHSS and Digital Modulation Techniques, 15.249, and Europe EN 300 220.



APPLICATIONS

- Garage Door Openers
- Low-Cost Consumer Electronic Applications
- Remote Keyless Entry (RKE)
- Remote Control / Security Systems

KEY PRODUCT FEATURES

- +10 dBm or 0 dBm Configurable output power
- Bit rates up to 100 kbps
- OOK and FSK modulation.
- 1.8 to 3.7 V supply range.
- Low BOM Fully Integrated Tx
- Fractional-N PLL with 1.5 kHz typical step
- Frequency agility for FHSS modulation
- FCC CFR Part 15.247 Digital Modulation Techniques

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This product datasheet contains a detailed description of the HC1243 performance and functionality.

1 Circuit Description

1.1 General Description

The HC1243 is a fully-integrated multi-band, single chip transmitter IC capable of FSK and OOK modulation of an input data stream.

It contains a frequency synthesizer which is a fractional-N sigma-delta PLL. For frequency modulation (FSK), the modulation is made inside the PLL bandwidth. For amplitude modulation (OOK), the modulation is performed by turning on and off the output PA.

The frequency reference used by the PLL is generated by a 22, 24 or 26 MHz crystal oscillator, depending on the frequency band of interest.

The Power Amplifier (PA), connected to the RFOUT pin, can deliver 0 dBm or +10 dBm in a 50 ⏜ load. Each of these two output powers need a specific matching network when efficiency needs to be optimized.

The circuit can be configured via a simplified TWI interface, constituted of pin CTRL and DATA. The pins of this interface are also used to transmit the modulating data to the chip.

Another key feature of the HC1243 is its low current consumption in Transmit and Sleep modes and its wide voltage operating range from 1.8 V to 3.7 V. This makes the HC1243 suitable for low-cost battery chemistries or energy harvesting applications.

1.2 Block Diagram

The figure below shows the simplified block diagram of the HC1243.

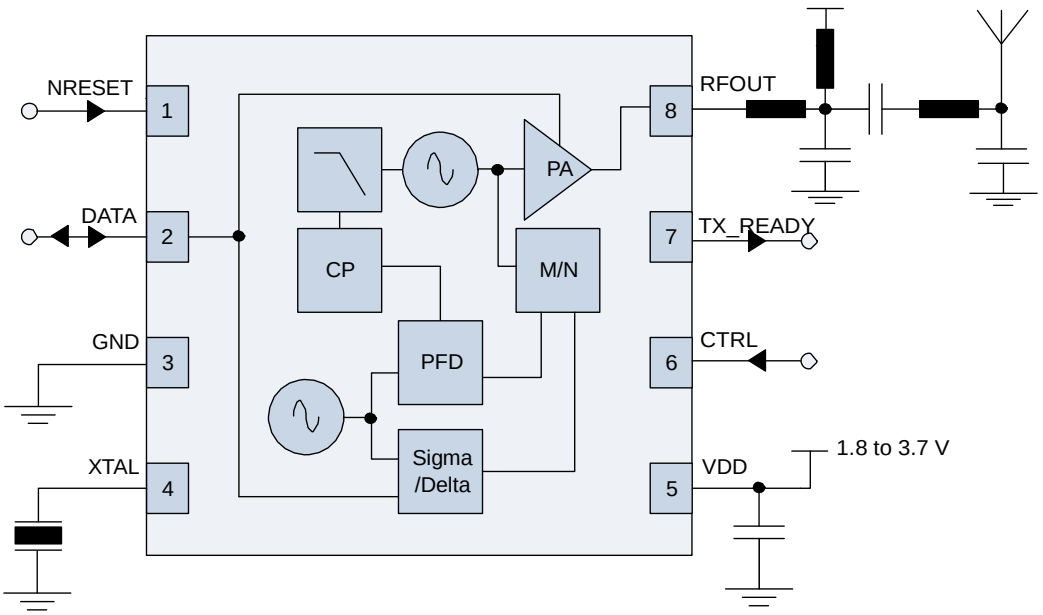


Figure 1. HC1243 Simplified Block Diagram

1.3 Pin Configuration

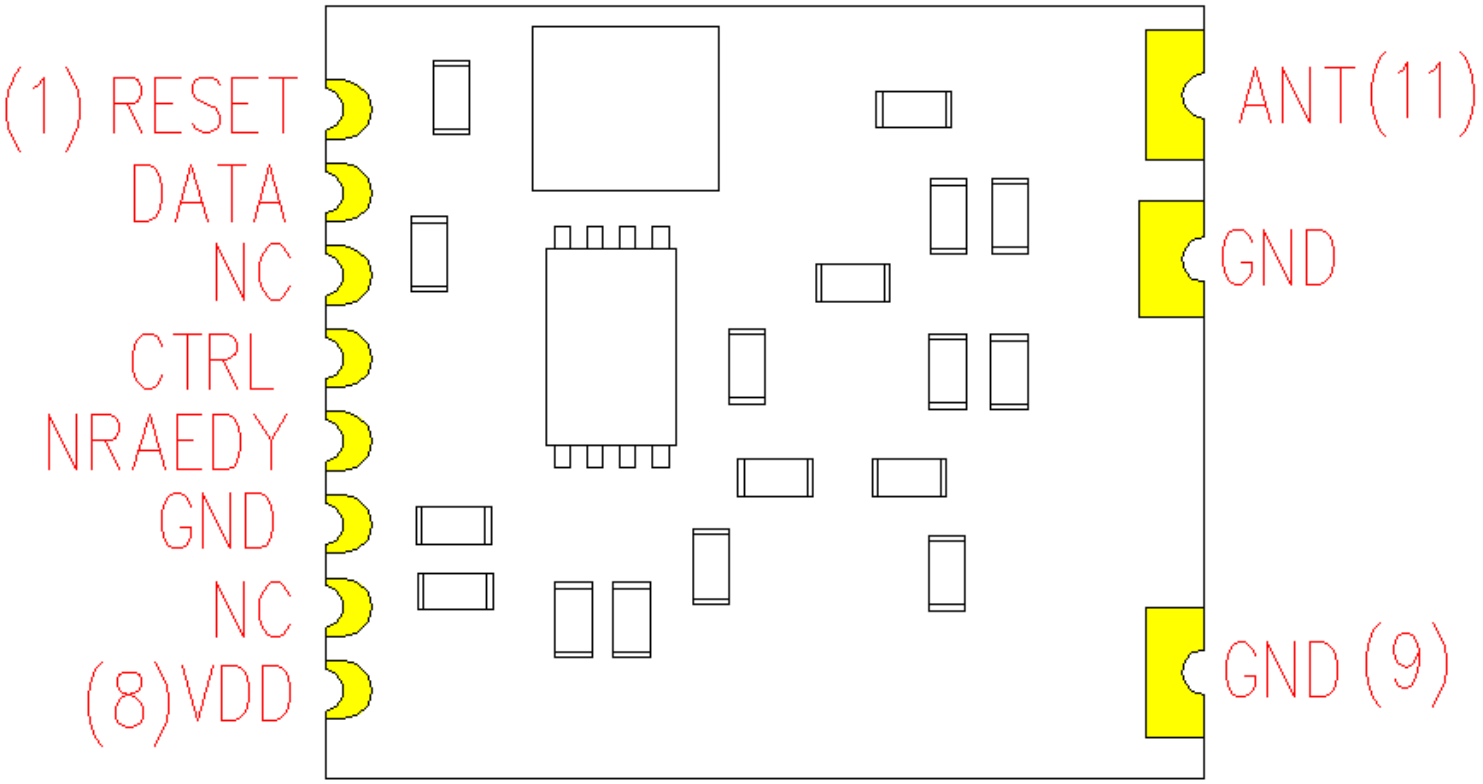


Figure 2. Pin Configuration

Table 1: Pinout Overview

PIN No.	Name	I/O	Description
1	RESET	I	Module Hardware Reset, low pulse active
2	DATA	I/O	Transmit Data Transmit or Configuration Data
3	NC		Not connection
4	CRT	I	Config Selection Configuration Data Clock
5	NRAEDY	O	Transmitter Ready Flag (Optional, can be left floating)
6	GND	I	Module Power supply Negative, Ground
7	NC		Not connection
8	VDD	I	Module Power supply Positive
9	GND	I	Module Power supply Negative, Ground
10	GND	I	Module Power supply Negative, Ground
11	ANT	O	Module RF Output

2 Electrical Characteristics

2.1 ESD Notice

The HC1243 is an electrostatic discharge sensitive device. It satisfies Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model) on all pins.

2.2 Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	115	° C
Tjunc	Junction Temperature	-55	125	° C
Tstor	Storage Temperature	-55	150	° C

2.3 Operating Range

Operating ranges define the limits for functional operation and the parametric characteristics of the device as described in this section. Functionality outside these limits is not implied.

Table 3 Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.7	V
Top	Operational temperature range	-40	85	° C
Clop	Load capacitance on digital ports	-	25	pF

2.4 Electrical Specifications

The table below gives the electrical specifications of the transmitter under the following conditions: Supply voltage VBAT = 3.3 V, temperature = 25 °C, f_{XOSC} = 26 MHz, f_{RF} = 915 MHz, 2-FSK modulation with Fdev=+/-10 kHz, bit rate = 10 kbit/s and output power = +10 dBm terminated in a matched 50 Ohm impedance, unless otherwise specified.

Table 4 Transmitter Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Current Consumption						
IDDSL	Supply current in Sleep mode		-	125		nA
IDDT_315	Supply current in Transmit mode at 315 MHz*	RFOP=+10dBm 50% OOK RFOP=+10dBm FSK RFOP=0dBm FSK	- - -	11 15 9	- - -	mA mA mA
IDDT_915	Supply current in Transmit mode at 915 MHz*	RFOP=+10dBm FSK RFOP=0dBm FSK	- -	17.5 10.5	- -	mA mA
RF and Baseband Specifications						
FBAND	Accessible Frequency Bands See details in Table 7.	Band 0, with FXOSC=22 MHz	310	-	450	MHz
		Band 0, with FXOSC=24 MHz	312	-	450	MHz
		Band 0, with FXOSC=26 MHz	338	-	450	MHz
		Band 1, with FXOSC=26 MHz	860 902	- -	870 928	MHz MHz
FDA	Frequency deviation, FSK		10	-	200	kHz
BRF	Bit rate, FSK	Permissible Range	0.5	-	100	kbps
BRO	Bit rate, OOK	Permissible Range	0.5	-	10	kbps
OOK_B	OOK Modulation Depth		-	45	-	dB
RFOP	RF output power in 50 Ohms in either frequency band	High Power Setting Low Power Setting*	7 -3	10 0	- -	dBm dBm
RFOPFL	RF output power flatness	From 315 to 390 MHz, 50 Ohms load	-	2	-	dB
DRFOPV	Variation in RF output power with supply voltage	2.5 V to 3.3 V 1.8 V to 3.7 V	- -	- -	3 7	dB dB
PHN	Transmitter phase noise	At offset: 100 kHz 350 kHz 550 kHz 1.15 MHz	- - - -	-84 -94 -96 -105	- - - -	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
STEP_22	RF frequency step	FXOSC = 22 MHz, Band 0	-	1.34277	-	kHz
STEP_24	RF frequency step	FXOSC = 24 MHz, Band 0	-	1.46484	-	kHz
STEP_26	RF frequency step	FXOSC = 26 MHz, Band 0 FXOSC = 26 MHz, Band 1	- -	1.58691 3.17383	- -	kHz kHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
FXOSC	Crystal Oscillator Frequency		- - -	22 24 26	- - -	MHz MHz MHz
DFXOSC	Frequency Variation of the XOSC	No crystal contribution	-	-	+/-25	ppm
Timing Specifications						
TS_TR	Time from Sleep to Tx mode	XTAL dependant, with spec'd XTAL	-	650	2000	us
TS_HOP0	Channel hop time in Band 0	315 to 390 MHz	-	250	500	us
TS_HOP1	Channel hop time in Band 1	Maximum hop of 26 MHz***	-	200	400	us
TOFFT	Timer from Tx data activity to Sleep	Programmable	- -	2 20	- -	ms ms
RAMP	PA Ramp up and down time		-	20	-	us
T_START	Time before CTRL pin mode selection.	Time from power on to sampling of CTRL **	-	200 us + TS_OSC	-	ms

* *With different matching networks*

** *The oscillator startup time, TS_OSC, depends on the electrical characteristics of the crystal*

*** *From the last CTRL falling edge of the Frequency change instruction to transmitter ready (PA ramp up finished)*

3 Digital Specification

The following table gives the operating specifications for the digital inputs and outputs of the HC1243.

Table 5 Digital Signals Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VBAT
V_{IL}	Digital input level low		-	-	0.2	VBAT
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VBAT
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VBAT
f_{CTRL}	CTRL Clock Frequency		-	-	10	MHz
t_{ch}	CTRL Clock High time		45	-	-	ns
t_{cl}	CTRL Clock Low time		45	-	-	ns
t_{rise}	CTRL Clock rise time		-	-	5	ns
t_{fall}	CTRL Clock Fall time		-	-	5	ns
t_{setup}	DATA Setup time	From Data transition to CTRL rising edge	45	-	-	ns
t_{hold}	DATA hold time	From CTRL rising edge to DATA transition	45	-	-	ns
t_0, t_2	Time at “1” on DATA during Recovery command	See Figure 10 and Figure 11	-	-	5	us
t_1	Time at “0” on DATA during Recovery command	See Figure 11	5	-	-	us

4 Application Modes of the HC1243

Pins CTRL and DATA are used for both configuring the circuit and sending the data to be transmitted over the air. Two different modes are associated to these pins, "**Power&Go**" and "**Advanced**" modes.

4.1 Transmitter Modes

Automatic Mode operation is described in Figure 3. Here we see that a rising edge on the DATA pin activates the transmitter start-up process. DATA must be held high for the start-up time (TS_TR) of the HC1243. During this time the HC1243 undergoes an optimized, self-calibrating trajectory from Sleep mode to Transmit mode. Once this time has elapsed, the HC1243 is ready to transmit. Any logical signal subsequently applied to the DATA pin is then transmitted.

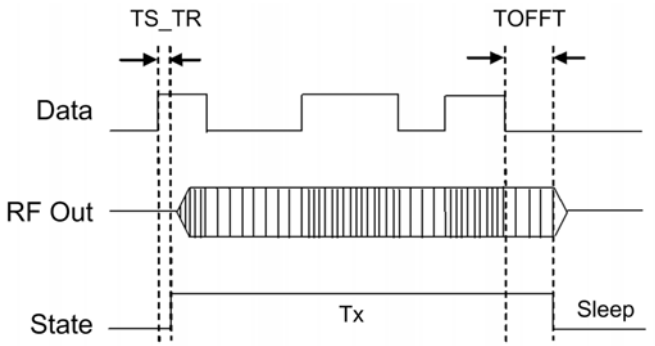


Figure 3. 'Power & Go' Mode: Transmitter Timing Operation

The transition back to Sleep mode is managed automatically. The HC1243 waits for TOFFT (2 or 20 ms) of inactivity on DATA before returning to Sleep mode.

In **Forced Transmit Mode** the circuit can be forced to wake up and go to TX mode by sending an APPLICATION instruction through the TWI interface, and setting the Mode bit DA(15) to '1'. Once in Transmit the circuit will transmit over the air the data stream presented on the DATA pin. The circuit will stay in transmit mode until a new APPLICATION instruction is sent with DA(15) to '0'.

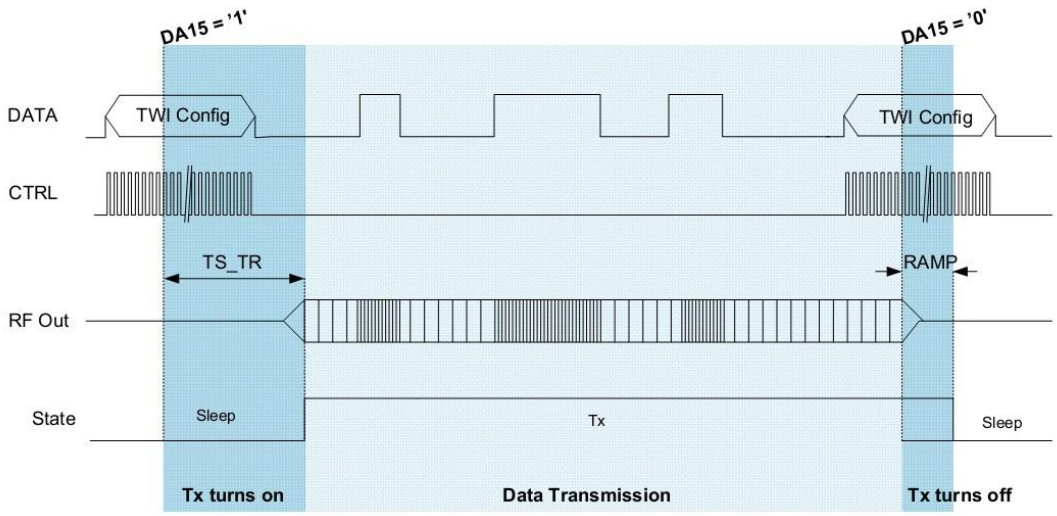


Figure 4. Forced Transmit Mode Description

4.2 Mode Selection Flowchart

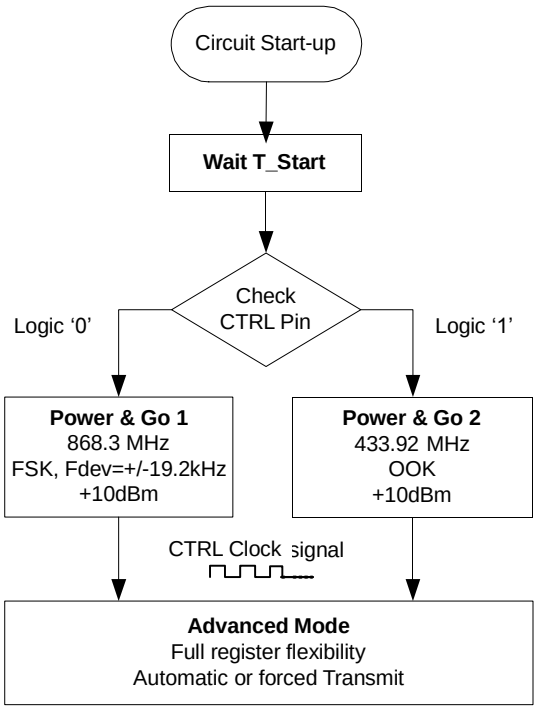


Figure 5. HC1243 Mode Selection

Note: Advanced mode is entered only if DATA is held low during CTRL's rising edge.

When powering up the circuit (microcontroller and HC1243), the logic level of the CTRL pin is sampled after T_START, as described on Figure 6. During T_START, the microcontroller IO driving the CTRL pin must be configured as an output, driving the CTRL pin to the desired state.

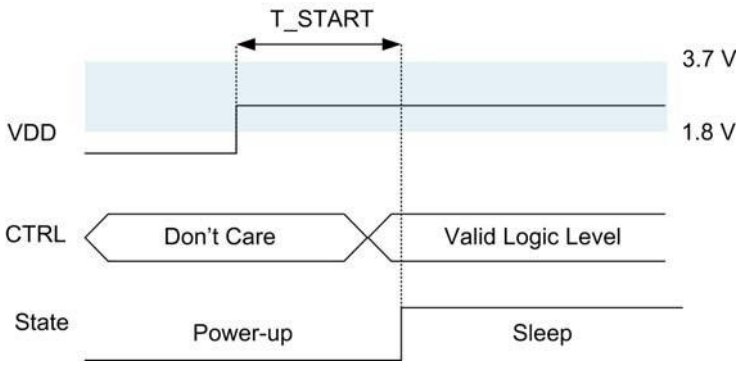


Figure 6. Power-up Timing

4.3 Application Mode: Power & Go

The default 'Power & Go' application mode sees the HC1243 configured as detailed in Table 6. By changing the logical state of the CTRL pin at Power-up or Reset, two distinct configuration modes can be selected. The Power & Go application modes hence permit microcontroller-less operation.

Table 6 Configuration in Power & Go Mode

CTRL Pin	Configuration	Mode
'Low'	FSK 868.3 MHz, +10 dBm, Fdev=+/-19.2 kHz	**Power&Go 1**
'High'	OOK 433.92 MHz, +10 dBm	**Power&Go 2**

4.4 Application Mode: Advanced

4.4.1 Advanced Mode: Configuration

As described on Figure 5, Advanced mode is entered when accessing the Two Wire Interface (TWI) bus of the HC1243. Upon communication to the register at up to 10 MHz of clocking speed, complete flexibility on the use of the chip is obtained.

Once all register settings are selected (see registers detailed description in section [5]), the HC1243 can be used either in Automatic mode by simply toggling the DATA pin, or in Forced Transmit mode to optimize timings for instance.

4.4.2 Frequency Hopping Spread Spectrum

Frequency hopping is supported in Advanced mode. After sending the data stream in the first channel, the user can send a Frequency change instruction containing the new channel frequency. The circuit will automatically ramp down the PA, lock the PLL to the new frequency, and turn the Power Amplifier back on. The user can then send his packet data on the new channel. Timings are detailed hereafter:

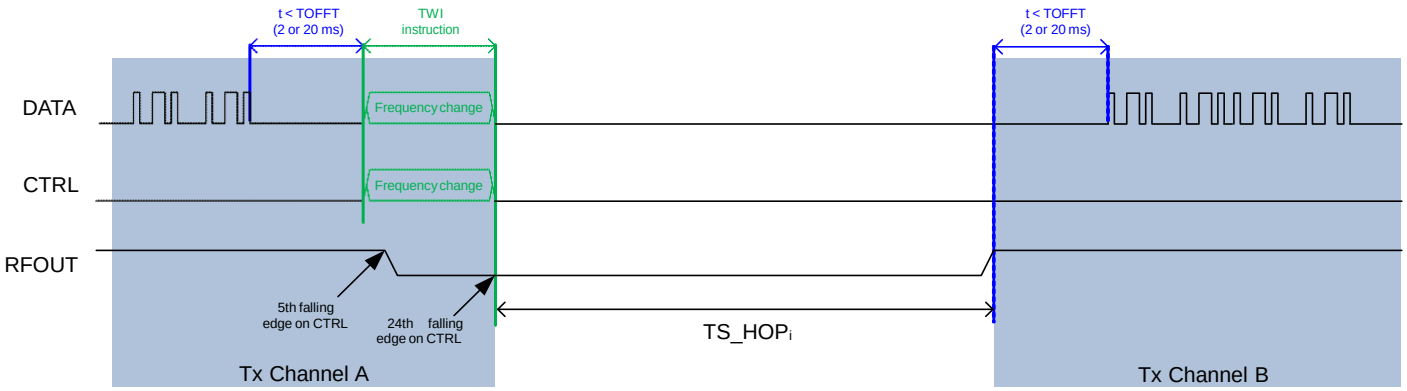


Figure 7. Frequency Hopping Description

Notes: - During any TWI access, the input of the modulator is inhibited

- The time between two Frequency change instructions shall be greater than TS_HOPi

- FHSS modulation, as described under FCC part 15.247, is supported by the HC1243; also note that the large Frequency Deviation settings available on the HC1243 make it suitable for "Digitally Modulated Systems", as described under FCC Part 15.247 (a)(2)

4.5 Frequency Band Coverage

The HC1243 offers several combinations or frequency references and frequency outputs, allowing for maximum flexibility and design of multi-band products:

Table 7 Frequency Selection Table

Reference Frequency FXOSC	Band Setting DA(13)	Upper / Lower Frequency Bounds	Fstep	Frf & Fdev
22 MHz	0	**310 to 450 MHz**	$Fstep = \frac{22x10^6}{2^{14}} = 1.34277kH$	$Frf = DF(18;0) \times Fstep$ $Fdev = DA(12;5) \times Fstep$
24 MHz		**312 to 450 MHz**	$Fstep = \frac{24x10^6}{2^{14}} = 1.46484kHz$	
26 MHz		**338 to 450 MHz**	$Fstep = \frac{26x10^6}{2^{14}} = 1.58691kHz$	
	1	**860 to 870 MHz and 902 to 928 MHz**	$Fstep = \frac{26x10^6}{2^{13}} = 3.17383kHz$	

4.6 Power Consumption

The following typical power consumption figures are observed on the HC1243 kits. Note that the transmitter efficiency depends on the impedance matching quality, and can be PCB design dependant.

The PA matching may be different in each frequency band.

Table 8 Power Consumption in Tx mode

Frequency Band	Conditions	Typical Current Drain
310 to 450 MHz	Pout=+10dBm, OOK modulation with 50% duty cycle Pout=+10dBm, FSK modulation Pout=0dBm, FSK modulation	11 mA 15 mA 9 mA
860 to 870 MHz	Pout=+10dBm, FSK modulation Pout=0dBm, FSK modulation	16.5 mA 10 mA
902 to 928 MHz	Pout=+10dBm, FSK modulation Pout=0dBm, FSK modulation	17.5 mA 10.5 mA

5 HC1243 Configuration

The HC1243 has several configuration parameters which can be selected through the serial interface.

5.1 TWI Access

As long as CTRL is kept stable, the DATA pin is considered by the circuit as the input for the data to be transmitted over the air (Power&Go modes).

Programming of the configuration register is triggered by a rising edge on the CTRL line. Upon detection of this rising edge, the data applied to the DATA pin is accepted as register configuration information, the data bits are clocked on subsequent rising edges of the clocking signal applied to the CTRL pin. The timing for HC1243 configuration register 'write' is shown in Figure 8. Note that, once triggered, all 24 clock cycle must be issued to the HC1243.

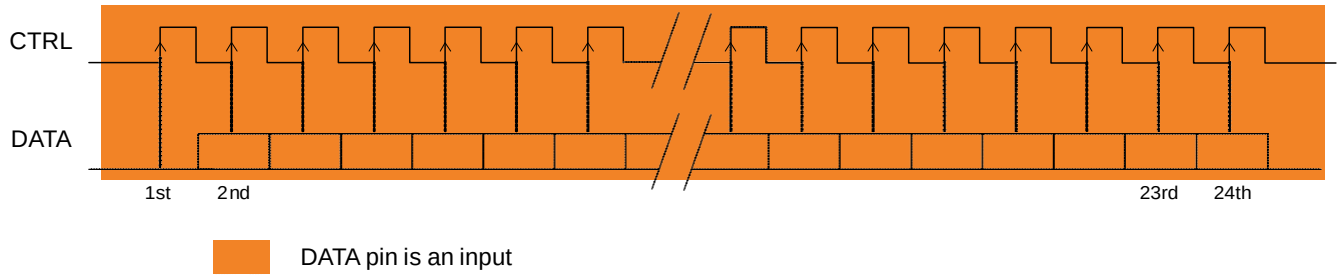


Figure 8. TWI Configuration Register 'Write'.

The registers may, similarly, be read using the timing of Figure 9.

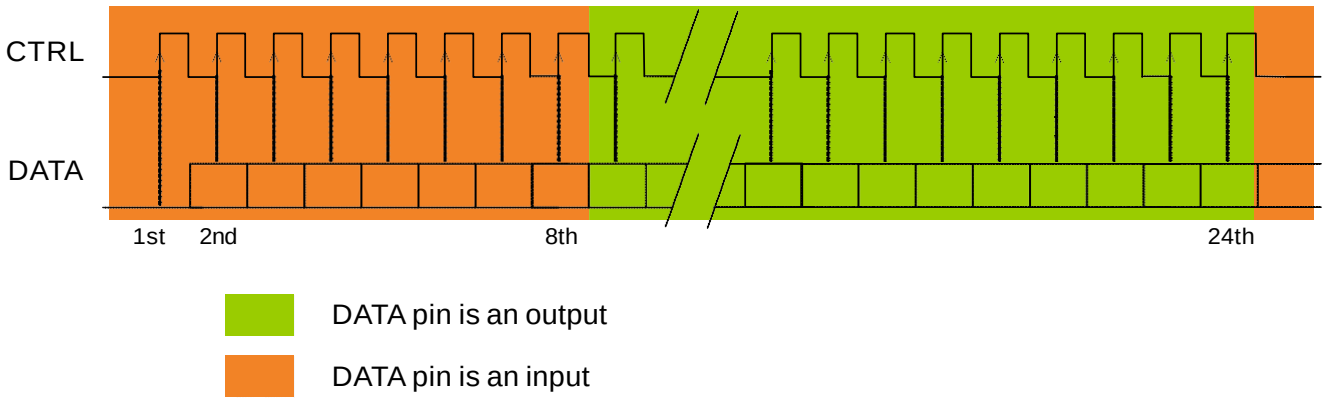


Figure 9. TWI Configuration Register 'Read'.

The first rising edge on CTRL which initiates the ADVANCED mode must occur at least 1 ms after the circuit has been powered up or reset.

Table 9 TWI Instruction Table

Byte 0								Byte 1								Byte 2								Instruction
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	0	0	0	(0000)				DA(15:0)																**Write** Application bits
0	0	0	1	1	DF(18:0)																			**Write** Frequency bits
0	0	1	0	(0)(0010)(0010)								DT(10:0)												**Write** Test bits (pad protected)
0	0	1	1	(0011)				DA(15:0)																**Read** Application bits
0	1	0	0	(0100)				DF(15:0)																**Read** the 16 least significant Frequency bits
0	1	0	1	(0101)				DS(12:5)								DS(4:0)					DF(18:16)			**Read** Chip version, Status and 3 most significant Frequency bits
0	1	1	0	(0110)				DS(28:13)																**Read** Bist signature
0	1	1	1	(0111)				(1111)(1)								DT(10:0)								**Read** Test bits
1	x																							**Discarded**, not an instruction
All 1																								**Recovery** instruction

Notes - The first "0" transmitted to the HC1243 is required to initialize communication

- The following 3 bits (highlighted in blue) determine the Typ of instruction

- The forthcoming bits (highlighted in green) define a protection pattern; any error in these bits voids the instruction

5.2 APPLICATION Configuration Parameters

Table 10 APPLICATION Configuration Parameters

Name	Number	Description	Power &Go 1	Power &Go 2
Mode	DA(15)	Mode: 0 ◎ Automatic mode 1 ◎ Forced transmit mode	0	
Modul	DA(14)	Modulation scheme: 0 ◎ FSK 1 ◎ OOK	0	1
Band	DA(13)	Band 0, 310 to 450 MHz Band 1, 860 to 870 MHz and 902 to 928 MHz	1	0
Fdev	DA(12:5)	RF Frequency deviation in FSK mode only See Table 7 for details	0x06 Fdev= +/-19.2kHz	Unused
Pout	DA(4)	Output power range: 0 ◎ 0 dBm 1 ◎ 10 dBm	1	1
TOFFT	DA(3)	Period of inactivity on DATA before HC1243 enters Sleep mode in Automatic mode: 0 ◎ 2 ms 1 ◎ 20 ms	0	1
RES	DA(2:0)	Reserved	100	100

Note: All changes to the APPLICATION parameters must be performed when the device is in Sleep mode, with the exception of DA(15). Mode can be sequentially written to "1", and then "0" while the device is in Transmit mode, to speed up the turn off process and circumvent the TOFFT delay.

5.3 FREQUENCY Configuration Parameters

Table 11 FREQUENCY Configuration Parameters

Name	Number	Description	Power &Go 1	Power &Go 2
Frf	DF(18:0)	RF operating frequency See Table 7 for details	0x42CAD Frf=868.3 MHz With 26 MHz reference	0x42C1C Frf=433.92 MHz With 26 MHz reference

If done in Sleep mode, the Frequency change instruction will be applied next time the HC1243 is turned on. If Frequency change occurs during transmission, the automated Frequency Hopping sequence described in section [4.4.2] will take place.

5.4 Test Parameters

Ten Test bits DT(9:0) exist in the HC1243. They are only use for the industrial test of the device, and therefore they are pad protected. It means that their value cannot be modified without applying a specific logical level to some of the HC1243 pads during a write access.

5.5 Status Parameters

DS(12:5) are read-only bits, organized as follows:

Table 12 Status Read-Only Parameters

Name	Number	Description	Default Advanced Mode	Power &Go 1	Power &Go 2
RES	DS(28:13)	Reserved	-		
Chip Version	DS(12:5)	Chip identification number	"0001 0001" --> V1A		
RES	DS(4:2)	Reserved	-		
TX_READY	DS(1)	TX_READY, see section [6.5.1] 0 ⓪ Transmitter not Ready 1 ⓪ Transmitter is Ready	-		
RES	DS(0)	Reserved	-		

5.6 Recovery Command

In the event of spurious activity (less than 24 clock cycles received) on the CTRL pin, control over the TWI interface can be recovered in two possible ways:

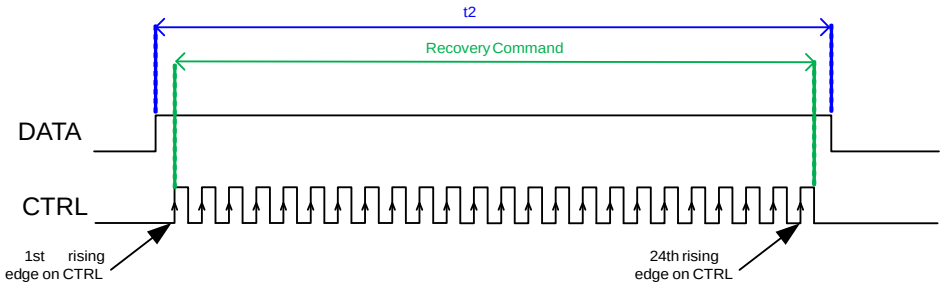


Figure 10. Quick Recovery Command

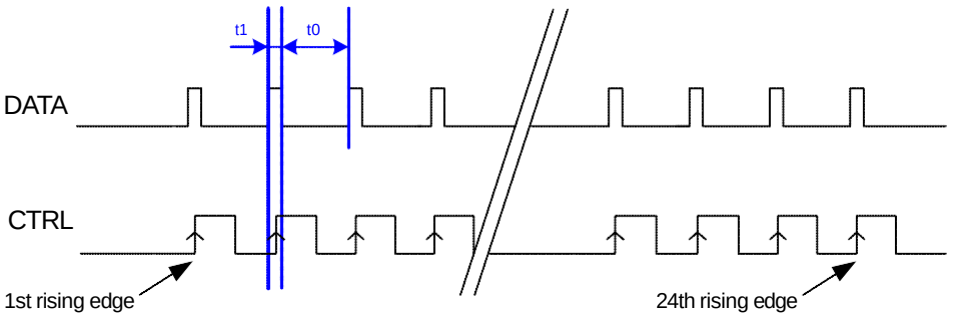


Figure 11. Pulsed Recovery Command

Notes - If t2 < 5 us, the HC1243 will not turn into Tx mode during the recovery command (if not previously in Tx mode)

- If t1 < 5 us, with t0 > 5 us, the HC1243 will not turn into Tx mode in the second scenario of recovery command

- During the Pulsed recovery command, t0 timing does not have any upper limit

- If t1 or t2 exceeds 5us, the recovery command will still be successful, but the transmitter will momentarily turn on

6 Application Circuit

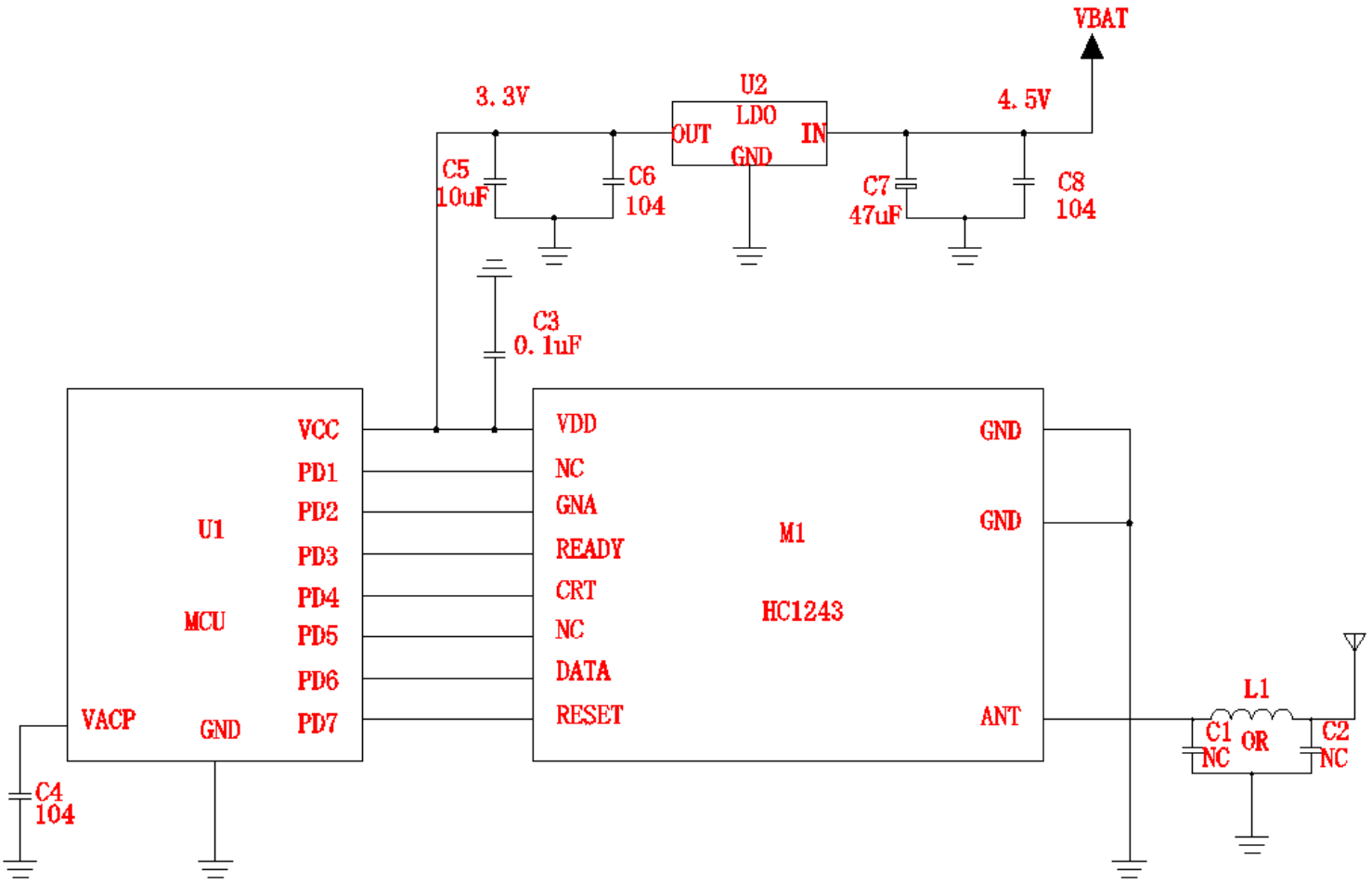
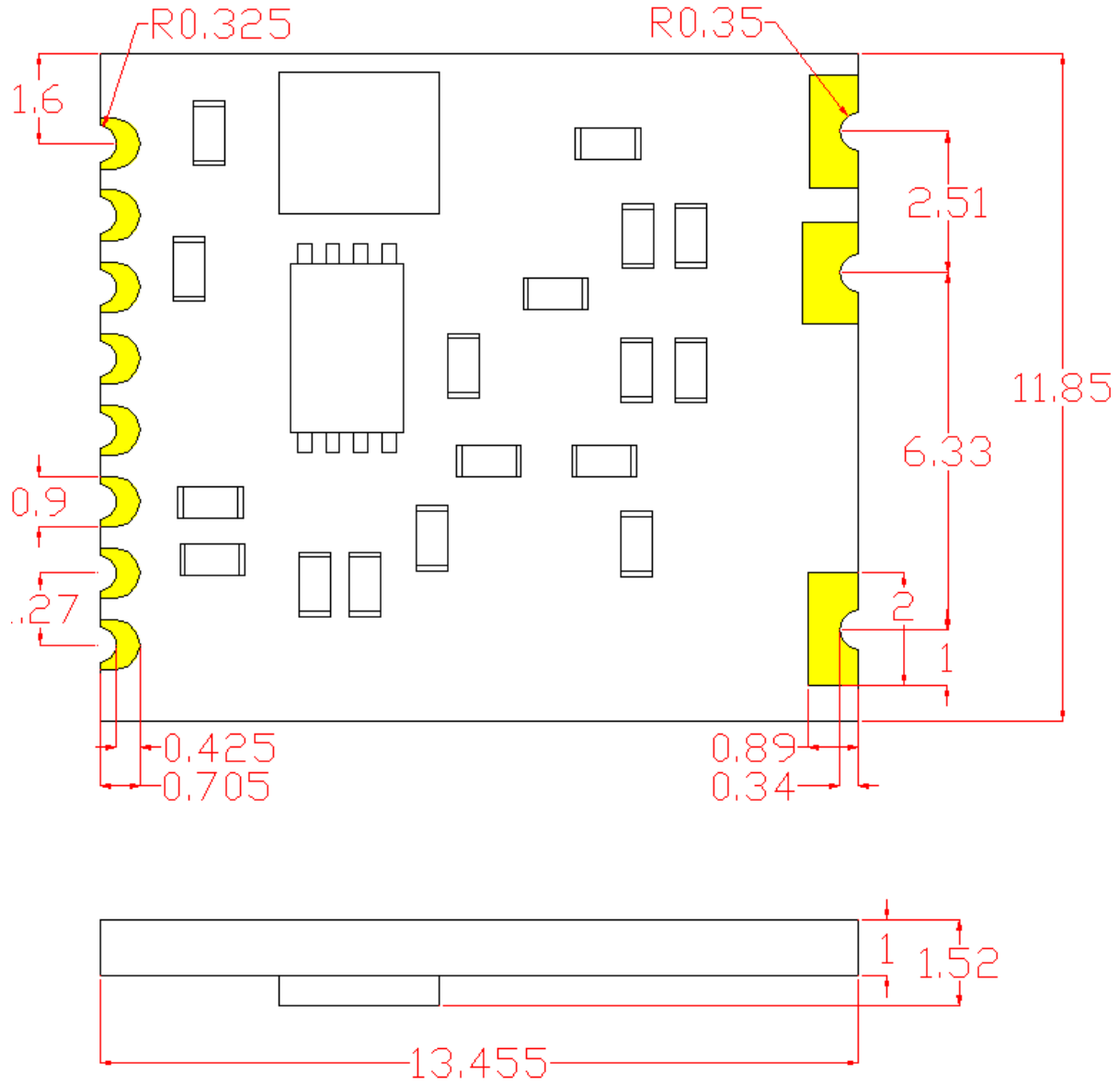


Table 13. BOM of Typical Application

Designator	Descriptions	Manufacturer
M1	Module HC1243 13.455*11.85*1.5mm RoHS	LJ ELECTRONICS
U1	IC 8 BIT MCU STM8S003F3 SSOP20 RoHS	MICROICHIP
U2	IC LDO XC6206P33PR 3.3V SOT-23 RoHS	TOREX
L1	Thick film resistor0R 5% 1/16W 0402 RoHS	ROHM
C1	CAP CER 0402 DO NOT FIT	
C2	CAP CER 0402 DO NOT FIT	
C3	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C4	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C5	CAP CER 10uF/16V 20% X5R 0402 RoHS	MURATA
C6	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C7	CAP CER 47uF/16V 20% X5R 1206 RoHS	MURATA
C8	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA

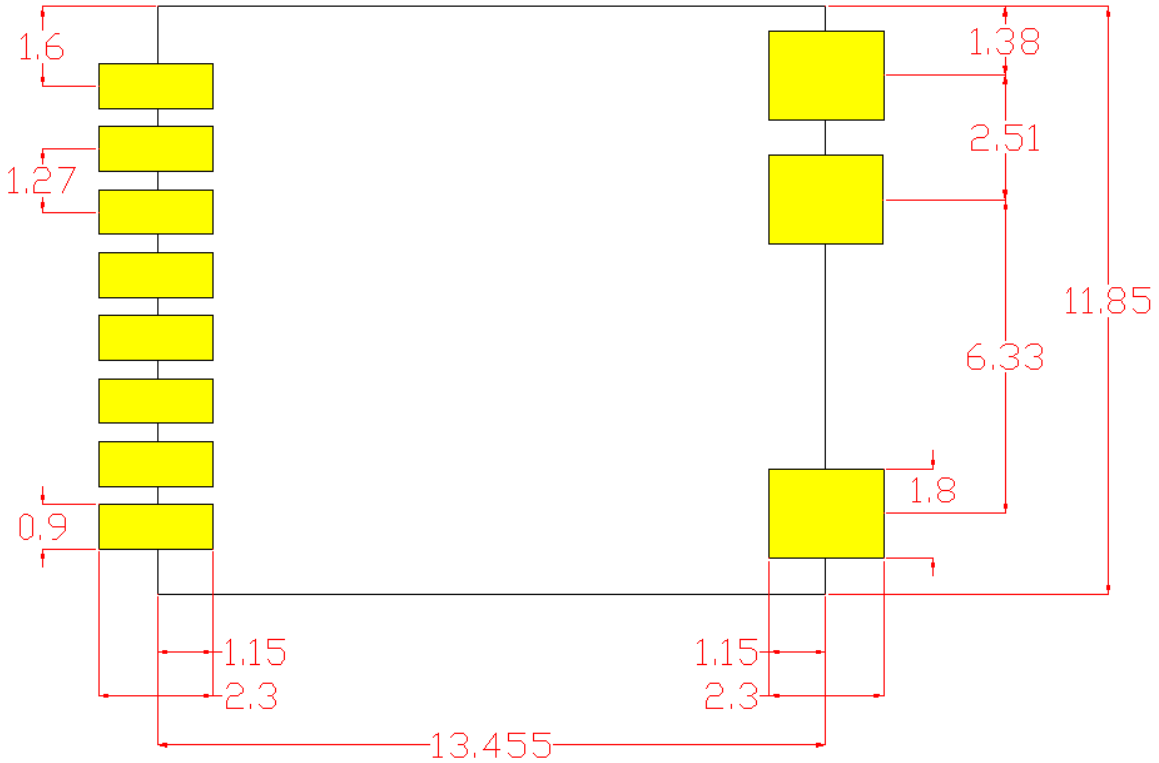
7 Module Package OutlineDrawing

Unit: mm



8 Recommended PCB Land Pattern

Unit: mm



9 Tray Packaging

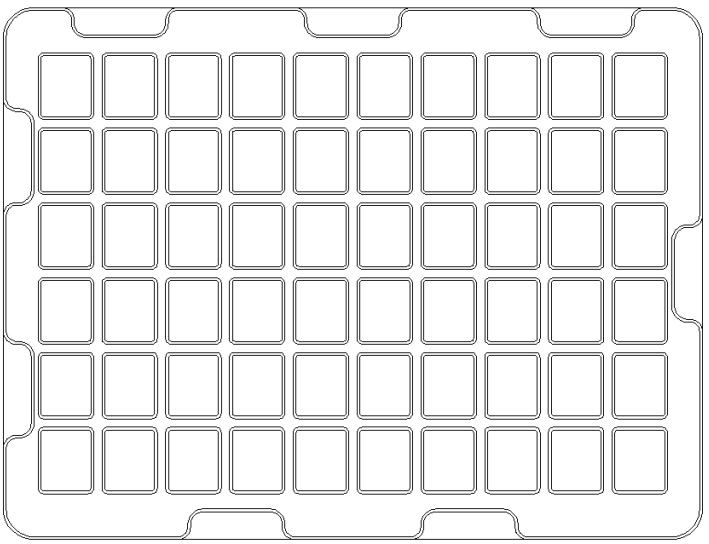
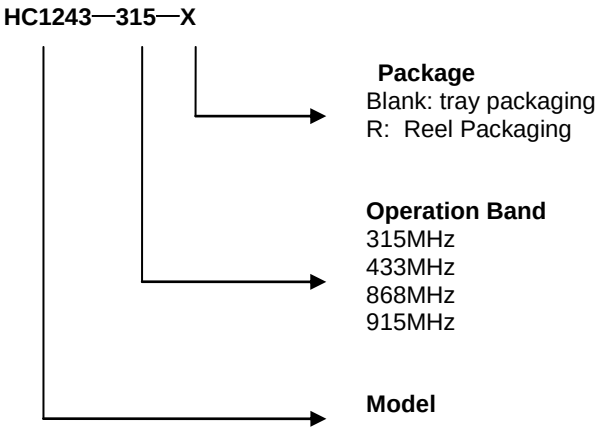


Figure 12. Package Outline Drawing

Note:

tray packaging, 60pcs/tray.

10 Ordering Information:



11 Module Revisions:

Table 14 Revision History

Revisions	Date	Updated History
Rev1.0	March 2014	The first final release
Rev1.1	June 2015	Update Module parameter for 868MHZ. 915MHZ
Rev1.2	April 2016	Add product pictures

12 Contact us:

LJ ELECTRONICS TECHNOLOGY LIMITED

Address: The 2nd Floor (west side),JieAn Industrial Park, The 1st Industrial Road,

TuTang Village,ChangPing Town,DongGuan City, GuangDong, China

TEL: 0769-81096302 0769-81096303 FAX: 0769-81096306

E-mail: sales@ljelect.com

Http://www. ljelect.com