Low Cost 2.4 GHz Radio Transceiver Module DATASHEET

GENERAL DESCRIPTION

The HC24GB is a low-cost, fully integrated CMOS RF transceiver module, GFSK data modem, and packet framer, optimized for use in the 2.4GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

The HC24GB transmits GFSK data at approximately 1 dBm output power. The low-IF receiver architecture produces good selectivity, with sensitivity down to approx. -87 dBm. Digital RSSI values are available to monitor channel quality.

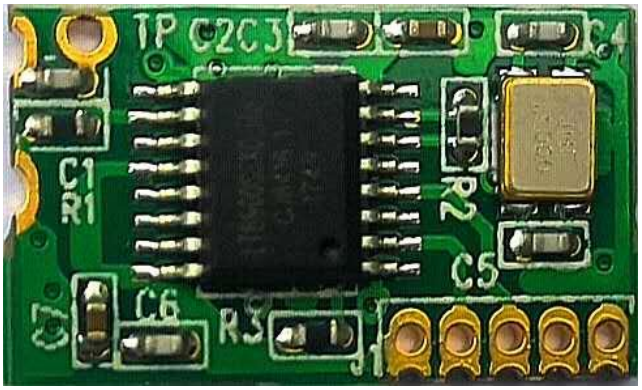
On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-airndata rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

The digital baseband interface can be either 4-wire SPI or 2-wire I2C-bus. Three additional pins are available for optional reset and buffer control.

For extended battery life, power consumption is minimized all key areas. A sleep mode is available to reduce standby current consumption to just 1 uA typ. while preserving register settings.

KEY PRODUCT FEATURES

Complete 2.4 GHz radio transceiver includes fully integrated RF PLL and channel filtering Supports Frequency-Hopping Spread Spectrum Supports I^2C bus interface Built-in smart auto-acknowledge Tx/Rx protocol simplifies usage Packet data rate 1 Mbps over-the-air FIFO flag signal permits continuous streaming data at 1 Mbps over-the-air Power management for minimizing current consumption
Digital readout of RSSI and temperature



APPLICATIONS

Remote controls
Wireless keyboards and mice
Proprietary Wireless Networks
Home automation
Commercial and industrial short-range wireless
Wireless voice, VoIP, Cordless headsets
Robotics and machine connectivity

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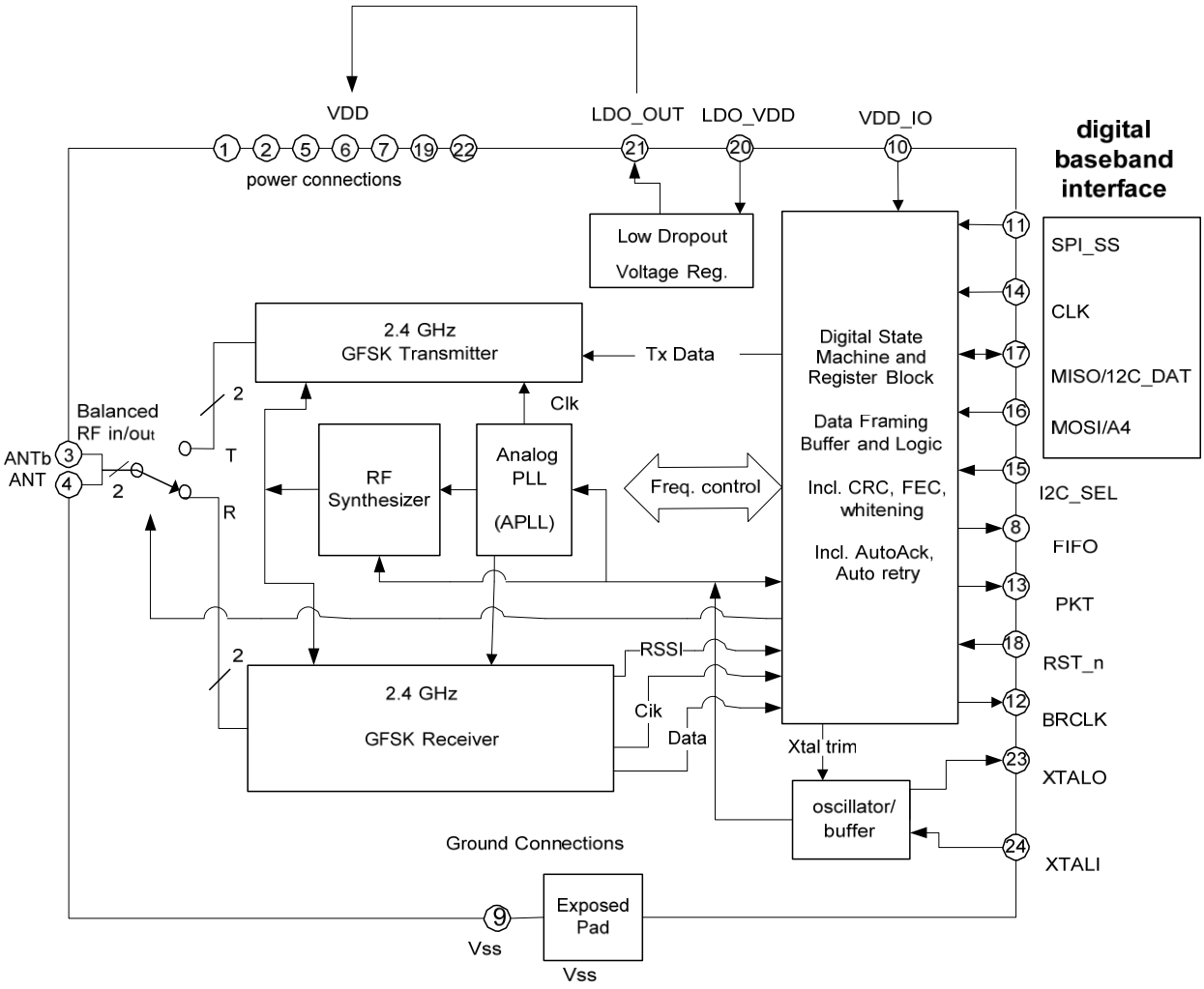
1 Block Diagram



2 Absolute Maximum Ratings

Table 1. Absolute Maximum Rating

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Temp.	T_{OP}	-40		+85	ºC
Storage Temp.	$T_{STORAGE}$	-55		+125	ºC
LDO_VDD, VDD_IO Voltage	V_{IN_MAX}			+3.7	VDC
VDD pins	VDD_MAX			+2.5	
Applied Voltages to Other Pins	V_{OTHER}	-0.3		+3.7	VDC
Input RF Level	P_{IN}			+10	dBm
Output Load mismatch (Z0=50Ω)	VSWROUT			10:1	VSWR

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.

2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

3 Electrical Characteristics

Table 2. Electrical Characteristics

The following specifications are guaranteed for TA = 25 C, LDO_VDD= VDD_IO = 3.3 VDC, unless otherwise noted.

Parameter	Symbol	MIN	TYP	MAX	Units	Test Condition and Notes
Supply Voltage						
DC power supply voltage range		1.9		3.6	VDC`	Input to VDD_IO and LDO_VDD pins.
Current Consumption						
Current Consumption - TX	IDD_TXH		18		mA	POUT = high power setting
	IDD_TXL		12		mA	POUT = low power setting
Current Consumption - RX	IDD_RX		17		mA	
Current Consumption –IDLE	IDD_IDLE1		1.4		mA	Configured for BRCLK output running.
	IDD_IDLE2		1.1		mA	Configured for BRCLK output OFF.
Current Consumption - SLEEP	IDD_SLP		1		uA	
Digital Inputs						
Logic input high	VIH	0.8 VDD_IN		1.2 VDD_IN	V	
Logic input low	VIL	0		0.8	V	
Input Capacitance	C_IN			10	pF	
Input Leakage Current	I_LEAK_IN			10	uA	
Digital Outputs						
Logic output high	VOH	0.8 VDD_IN		VDD_IN	V	
Logic output low	VOL			0.4	V	
Output Capacitance	C_OUT			10	pF	
Output Leakage Current	I_LEAK_OUT			10	uA	
Rise/Fall Time (SPI)	T_RISE_OUT			5	nS	
Clock Signals						
CLK rise, fall time (SPI)	Tr_spi			25	nS	Requirement for error-free register reading, writing.
CLK frequency range (SPI)	FSPI	0	12		MHz	
Overall Transceiver						
Operating Frequency Range	F_OP	2400		2482	MHz	
Antenna port mismatch	VSWR_I		<2:1		VSWR	Receive mode.
(Z0=50Ω)	VSWR_O		<2:1		VSWR	Transmit mode.

Parameter		Symbol	MIN	TYP	MAX	Unis		
Receive Section							BER≤0.1%	
Receiver sensitivity				-87		dBm		
Maximum useable signal			-20	1		dBm		
Data (Symbol) rate		Ts		1				
Min. Carrier/Interference ratio								
Adjacent Ch. Interference,1MHz offset		CI_1		+6		dB	-60 dBm desired signal.	
Adjacent Ch. Interference,2MHz offset		CI_2		-12		dB	-60 dBm desired signal.	
Adjacent Ch. Interference,3MHz offset		CI_3		-24		dB	-67 dBm desired signa	
Out-of-Band Blocking For additional test conditions, see footnote1.		OBB_1	-10			dBm	30 MHz to 2000 MHz	Meas. with ACX BF2520 ceramic filter 2 on ant. pin
		OBB_2	-27			dBm	2000 MHz to 2400 MHz	
		OBB_3	-27			dBm	2500 MHz to 3000 MHz	Desired sig. -67 dBm, BER ≤ 0.1%.
		OBB_4	-10			dBm	3000 MHz to 12.75 GHz	
Transmit Section							Measured using 50 Ohm balun3:	
RF Output Power		PAV			6	dBm	POUT= maximum output power Reg09=0x4000	
				2			POUT = nominal output power, Reg09=0x1840	
			-17				POUT=minimum output power,Reg09=1FC0	
Second harmonic				-50		dBm	Conducted to ANT pin.	
Third harmonic				-50		dBm	Conducted to ANT pin.	
Modulation Characteristics								
Peak FM Deviation	00001111 pattern	Δf1avg		280		kHz		
	01010101 pattern	Δf2max		225		kHz		
In-Band Spurious Emission								
2MHz offset		IBS_2			-40	dBm		
>3MHz offset		IBS_3			-60	dBm		
Out-of-Band Spurious Emission, Operation		OBS_O_1		< -60	-36	dBm	30 MHz ~ 1 GHz	
		OBS_O_2		-45	-30	dBm	1 GHz ~ 12.75 GHz, excludes desired signal and harmonics.	
		OBS_O_3		< -60	-47	dBm	1.8 GHz ~ 1.9 GHz	
		OBS_O_4		< -65	-47	dBm	5.15 GHz ~ 5.3 GHz	
Co-Channel Interference		CI_cochannel		+9		dB	-60 dBm desired signal.	

Note:

1. ***The test is run at one midband frequency, typically 2460 MHz. With blocking frequency swept in 1 MHz steps, up to 24 exception frequencies are allowed. Of these, no more than 5 shall persist with blocking signal reduced to -50dBm. For blocking frequencies below desired receive frequency, in-band harmonics of the out-of-band blocking signal are the most frequent cause of failure, so be sure blocking signal has adequate harmonic filtering.***
2. ***In some applications, this filter may be incorporated into the antenna, or be approximated by the effective antenna bandwidth.***
3. ***Transmit power measurement is corrected for insertion loss of Balun, in order to indicate the transmit power at the IC pins.***

Parameter	Symbol	MIN	TYP	MAX	Unit	Test Condition and Notes	
RF VCO and PLL Section							
Typical PLL lock range	FLOCK	2366		2516	MHz		
Tx, Rx Frequency Tolerance			--		ppm	Same as XTAL pins frequency tolerance	
Channel (Step) Size			1		MHz		
SSB Phase Noise			≤ -95		dBc/Hz	550kHz offset	
			≤ -115		dBc/Hz	2MHz offset	
Crystal oscillator freq. range (Reference Frequency)			12.000		MHz	Designed for 12 MHz crystal reference freq.	
Crystal oscillator digital trim range, typ.			±20		ppm	See Register 27 description. Amount of pull depends on crystal spec. and operating point.	
RF PLL Settling Time	THOP		75	150	uS	Settle to within 30 kHz of final value.	
Spurious Emissions	OBS_1		< -75	-57	dBm	30 MHz ~ 1 GHz	IDLE state, Synthesizer and VCO ON.
	OBS_2		-68	-47	dBm	1 GHz ~ 12.75 GHz	
LDO Voltage Regulator Section							
Dropout Voltage	Vdo		0.17	0.5	V	Measured during Receive state	

4 Application Circuit

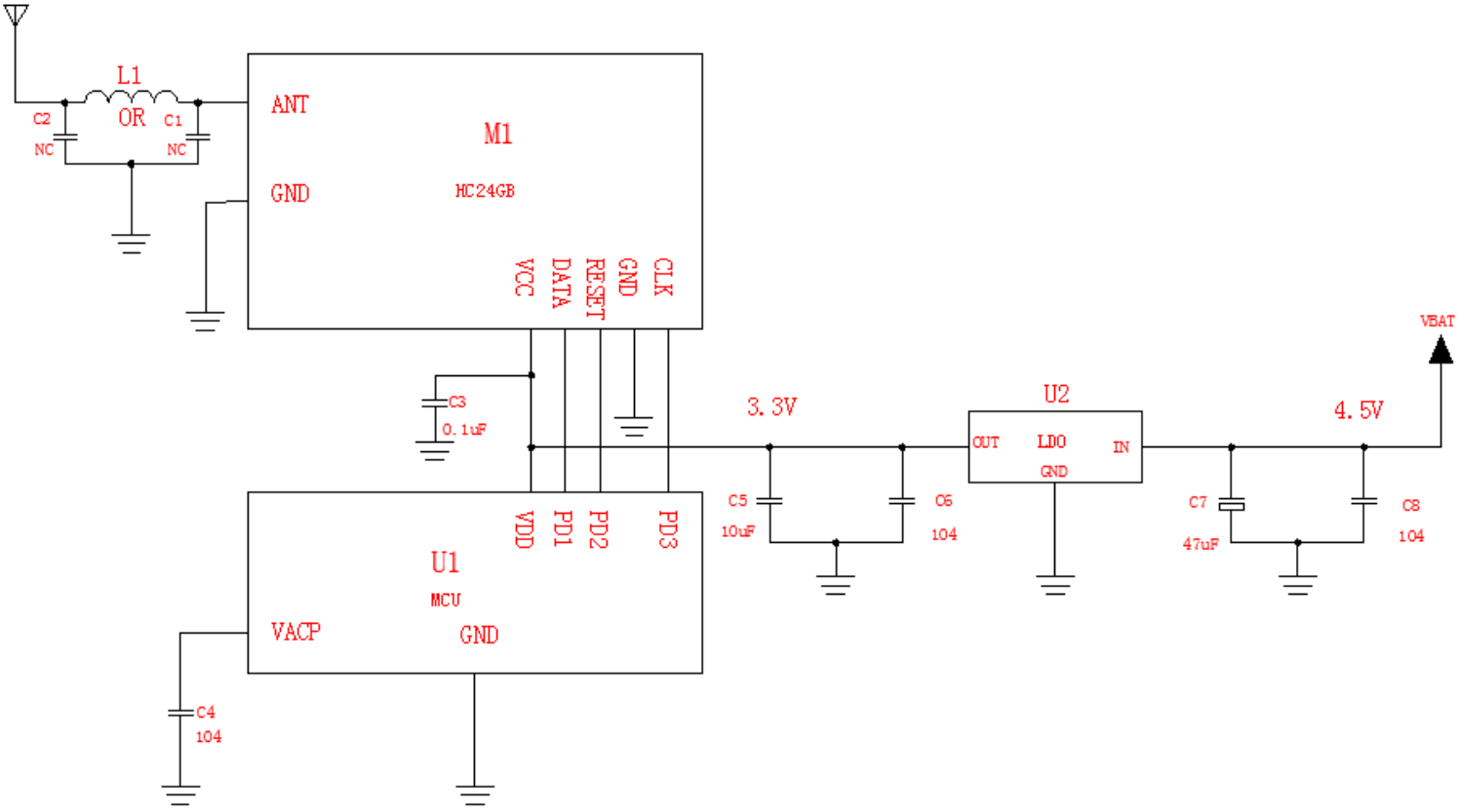


Table 3. BOM of Typical Application

Designator	Descriptions	Manufacturer
M1	Module HC24GB 15.91*9.55*1.64mm RoHS	LJ ELECTRONICS
U1	IC 8 BIT MCU STM8S003F3 SSOP20 RoHS	MICROICHIP
U2	IC LDO XC6206P33PR 3.3V SOT-23 RoHS	TOREX
L1	Thick film resistor0R 5% 1/16W 0402 RoHS	ROHM
C1	CAP CER 0402 DO NOT FIT	
C2	CAP CER 0402 DO NOT FIT	
C3	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C4	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C5	CAP CER 10uF/16V 20% X5R 0402 RoHS	MURATA
C6	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C7	CAP CER 47uF/16V 20% X5R 1206 RoHS	MURATA
C8	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA

5 Pin Description

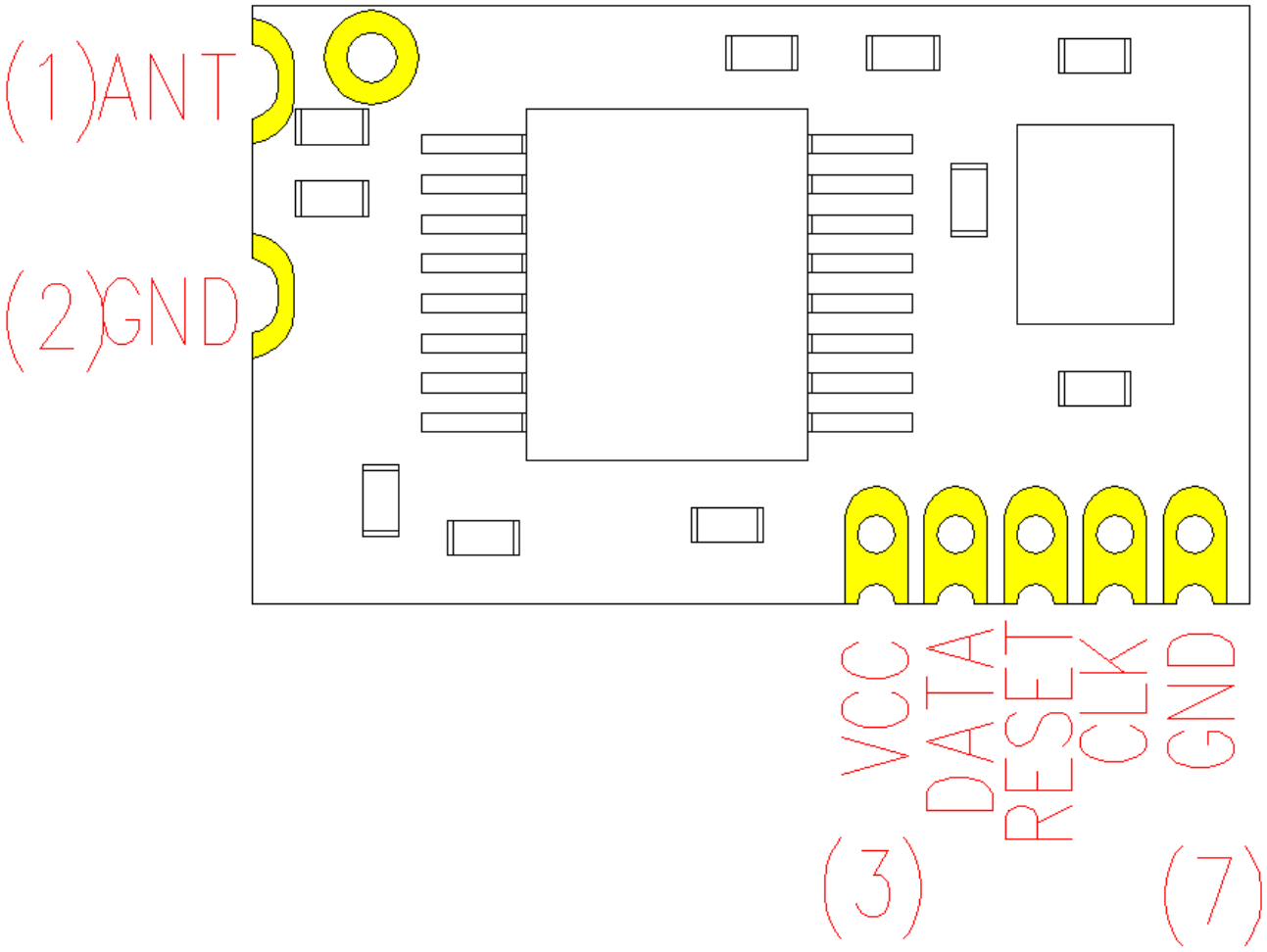


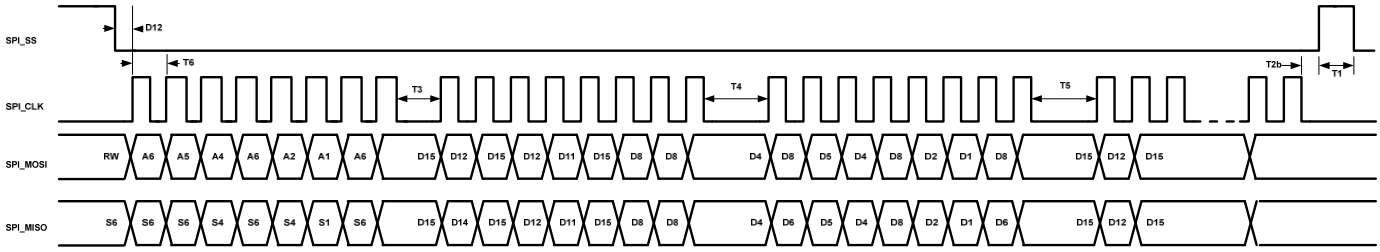
Table 4. Pin Description QFN24

PIN No.	Name	I/O/P	Description
1	ANT	O	Module antenna
2	GND	P	Module Power supply negative, ground.
3	VCC	P	Module Power supply Positive
4	DATA	I/O	Module I2C serial DATA.
5	RESET	I	Module Hardware Reset, low pulse active
6	CLK	I	Module I2C serial CLOCK
7	GND	P	Module Power supply negative, ground.

6 SPI Interface

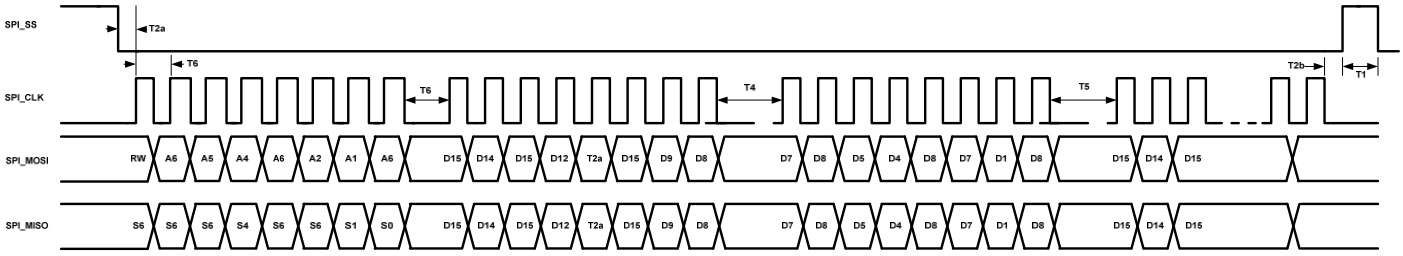
6.1 SPI Default Format

Figure 1. SPI Signal Format when CKPHA = 1 (Standard configuration for QFN packaged parts)



6.2 SPI Optional Format

Figure 2. SPI Signal Format when CKPHA = 0(For QFN packaged parts, this option available by special order only)



Notes:

1. Polarity of SPI read/write bit: Write= 0, Read= 1.

2. Access to FIFO Register 50 is byte-by-byte (always integer multiples of 8-bits). Access to multiple FIFO bytes may be combined into one or more SPI_SS cycle(s) if desired.

3. Access to all registers other than FIFO is always word length (16-bits per register).

4. Access to multiple registers (except FIFO register) may be combined into one SPI_SS cycle. If combined, address is written only once at the beginning of the SPI cycle, then each 16-bit register value follows. The HC24GB will auto-increment the register number that each word of data is placed into. If in doubt, simply use separate SPI_SS cycles for each 16-bit register write.

5. MISO return status byte S7:S0 will be the same as the top byte of Register 48 (contains result of CRC and FEC error check, and framer state status).

6.3 SPI Timing Requirements

Table 5. SPI Timing Requirements

Name	Min	Typ.	Max	Description
T1	250ns			Interval between two SPI accesses
T2a, T2b	41.5ns			Relationship between SPI_SS & SPI_CLK
T3	Note 1			Interval time between address and data
T4	Note 1			Interval time between high byte and low byte data
T5	Note 2			Interval time between two register data
T6	83ns			SPI_CLK period

Notes:

1. When MCU/application reads register 50 FIFO data, at least 450ns wait time is required for framer to get correct FIFO read point. For all other registers, T3min = 41.5ns.

2. When reading register 50 FIFO data, at least 450ns wait time is required.

For all other registers, T5min = 41.5ns.

7 IIC Interface

7.1 I2C Command Format

Figure 3. Example I2C Data Transfers

Example I2C Data Transfers:

Master write 1 or more data byes to LT8900 FIFO register:

Master writes 1 byte to LT8900 to specify FIFO register, then reads one or more bytes from LT8900 FIFO:

Master may continue reading LT8900 FIFO:

Sr: Repeated Start
A: Acknowledge

7.2 I2C Supported Features

Table 6. I2C Supported Feature List

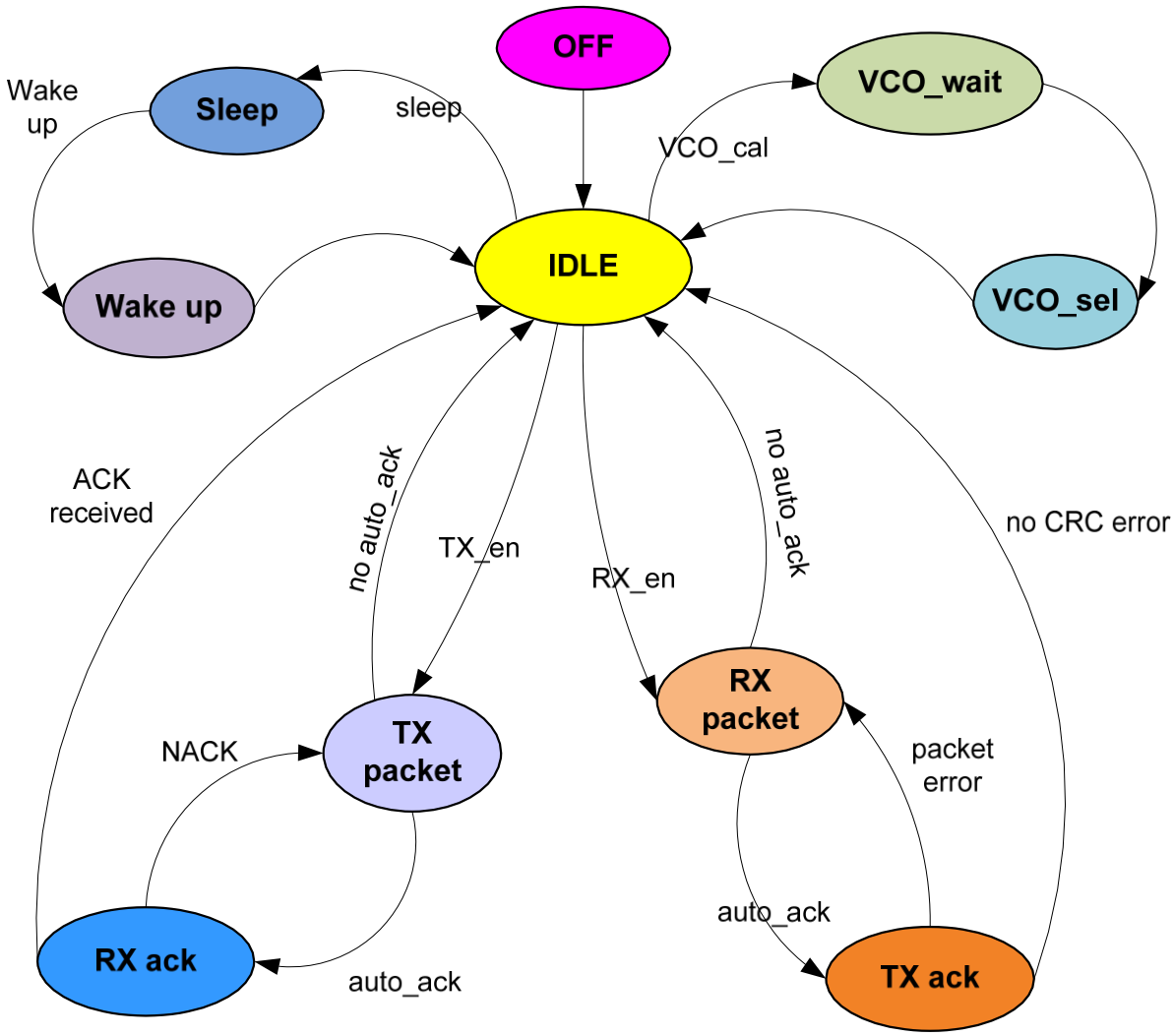
I2C device Slave Mode Optional Feature List	HC24GB Support?
Standard-mode – 100 kbps	Yes
Fast-mode – 400 kbps	Yes
Fast-mode Plus – 1000 kbps	Yes
High-speed mode – 3200 kbps	No
Clock Stretching	No
10-bit slave address	No
general call address	No
software reset	No
device ID	No

7.3 I2C Device Address

In I2C mode, the HC24GB responds to the following device address:

A6	A5	A4	A3	A2	A1	A0	R/W
0	Determined by bonding pad jumper. QFN packaged parts: Standard is '1'. Special order option is '0'. Bare Die: can be bonded however required.	Determined by bonding pad jumper. QFN packaged parts: As determined by pin 15, MOSI/A4. Bare Die: can be bonded however required.	1	0	0	0	Read=1 Write=0

8 Top Level State Diagram



9 Register Information

The following registers are accessed using SPI or I2C serial interface protocol.
Some of the internal registers and bit fields are not intended for end-user adjustment. Such registers are not described herein, and should not be altered from the factory-recommended value.

9.1 Register 3 – Read only

Table 7. Register 3 information

Bit No.	Bit Name	Description
15:13	(Reserved)	(Reserved)
12	RF_SYNTH_LOCK	Indicates the phase lock status of RF synthesizer. 1: Locked. 0: Unlocked.
11:0	(Reserved)	(Reserved)

9.2 Register 6 – Read only

Table 8. Register 6 information

Bit No.	Bit Name	Description
15:10	RAW_RSSI[5:0]	Indicate 4-bit raw RSSI values from analog circuit.
9:0	(Reserved)	(Reserved)

9.3 Register 7

Table 9. Register 7 information

Bit No.	Bit Name	Description
15:9	(Reserved)	(Reserved)
8	TX_EN	Initiate the Transmit Sequence for state machine control. Note that TX_EN and RX_EN cannot be “HIGH” at the same time.
7	RX_EN	Initiate the Receive Sequence for state machine control. Note that TX_EN and RX_EN cannot be “HIGH” at the same time.
6:0	RF_PLL_CH_NO [6:0]	This will be the 7 bit RF channel number. The on-air frequency will be: f = 2402 + RF_PLL_CH_NO.

9.4 Register 9

Table 10. Register 9 information

Bit No.	Bit Name	Description
15:12	PA_PWCTR[3:0]	PA current control
11	(Reserved)	(Reserved)
10:7	PA_GN[3:0]	4-bit power amplifier gain setting.
6:0	(Reserved)	(Reserved)

9.5 Register 10

Table 11. Register 10 information

Bit No.	Bit Name	Description
15:1	(Reserved)	(Reserved)
0	XTAL_OSC_EN	1: Enable crystal oscillator gain block. 0: Disable crystal oscillator gain block.

9.6 Register 11

Table 12. Register 11 information

Bit No.	Bit Name	Description
15:9	(Reserved)	(Reserved)
8	RSSI_PDN	1: Power down RSSI. 0: RSSI operates normally.
7:0	(Reserved)	(Reserved)

9.7 Register 23

Table 13. Register 23 information

Bit No.	Bit Name	Description
15:3	(Reserved)	(Reserved)
2	TxRx_VCO_CAL_EN	1: Calibrate VCO before each and every Tx/Rx enable. 0: Do not calibrate VCO before each and every Tx/Rx enable.
1:0	(Reserved)	(Reserved)

9.8 Register 27

Table 14. Register 27 information

Bit No.	Bit Name	Description
15:6	(Reserved)	(Reserved)
5:0	XI_trim[5:0]	Crystal frequency trim adjust.

9.9 Register 29 – Read only

Table 15. Register 29 information

Bit No.	Bit Name	Description
15:8	(Reserved)	(Reserved)
7:4	RF_VER_ID [3:0]	This field is used to identify minor RF revisions to the design.
3	(Reserved)	(Reserved)
2:0	Digital version	This field is used to identify minor digital revisions to the design.

9.10 Register 30 – Read only

Table 16. Register 30 information

Bit No.	Bit Name	Description
15:0	ID_CODE_L [15:0]	Lower bits of JEDEC JEP106-K Manufacture's ID code, containing manufacturer, part number, and version. The LSB is always "1".

9.11 Register 31 – Read only

Table 17. Register 31 information

Bit No.	Bit Name	Description
15:12	**RF_CODE_ID**	**JEDEC JEP106-K revision level.**
11:0	**ID_CODE_M [31:16]**	**Upper bits of Manufacture's ID code.**

9.12 Register 32

Table 18. Register 32 information

Bit	Name	R/W	Description	default
15:13	PREAMBLE_LEN	R/W	000: 1byte, 001: 2bytes, 010: 3 bytes, … 111: 8 bytes	010B
12:11	SYNCWORD_LEN	R/W	11: 64 bits {Reg39[15:0],Reg38[15:0],Reg37[15:0],Reg36[15:0]} 10: 48bits, {Reg39[15:0],Reg38[15:0],Reg36[15:0]} 01: 32bits, {Reg39[15:0],Reg36[15:0] 00: 16 bits,{Reg36[15:0]}	11B
10:8	TRAILER_LEN	R/W	000: 4 bits, 001: 6bits, 010: 8 bits, 011: 10 bits …. 111: 18 bits	000B
7:6	DATA_PACKET_TYPE	R/W	00: NRZ law data 01: Manchester data type 10: 8bit/10bit line code 11: Interleave data type	00B
5:4	FEC_TYPE	R/W	00: No FEC 01: FEC13 10: FEC23 11: reserved	00B

Bit	Name	R/W	Description	default
3:1	BRCLK_SEL	R/W	Selects output clock signal to BRCLK pin: 3'b000: keep low 3'b001: crystal buffer out 3'b010: crystal divided by 2 3'b011: crystal divided by 4 3'b100: crystal divided by 8 3'b101: TXCLK 1 MHz 3'b110: APLL_CLK (12 MHz during Tx, Rx) 3'b111: keep low	011B
0	(Reserved)	W/R	(Reserved)	0B

9.13 Register 33

Table 19. Register 33 information

Bit	Name	R/W	Description	default
15-8	VCO_ON_DELAY_CNT[7:0]	R/W	After set TX or RX wait delay timer for internal VCO setting time. Each time increment is 1 uS.	63H
7-6	TX_PA_OFF_DELAY[1:0]	R/W	Set PA off after PA_OFF command, 1 represents 1us, base is 4us	00B
5:0	TX_PA_ON_DELAY[5:0]	R/W	After set VCO_ON, it will wait this timer , than internal PA fully on,	07H

9.14 Register 34

Table 20. Register 34 information

Bit	Name	R/W	Description	default
15	Bpktctl_direct	R/W	When direct mode, it is used control PA on at TX and wide/narrow mode control at RX	0B
14-8	TX_CW_DLY[6:0]	R/W	Transmit CW modulation data at before transmit data, after PA on, continue TX CW mode time.	03H
7-6	Reserved	R/W		0B
5:0	TX_SW_ON_DELAY[5:0]	R/W	Set VCO_ON, wait this timer, internal TW switch turn on, 1 represents 1us	0BH

9.15 Register 35

Table 21. Register 35 information

Bit	Name	R/W	Description	default
15	POWER_DOWN	W	1: First set crystal off, then set LDO low-power mode (register values will be lost). 0: Leave power on.	0B
14	SLEEP_MODE	W	1: Enter SLEEP state (set crystal gain block to off. Keep LDO regulator on (register values will be preserved). Wakeup begins when SPI_SS goes low. This will restart the on-chip clock oscillator to begin normal operation. 0: Normal (IDLE) state.	0B
13	(Reserved)		(Reserved)	
12	BRCLK_ON_SLEEP	R/W	1: crystal running at sleep mode. Draws more current but enables fast wakeup. 0: crystal stops during sleep mode. Saves current but takes longer to wake up.	1B
11:8	RE-TRANSMIT_TIMES	R/W	Max. re-transmit packet attempts when auto_ack function is enabled.	3H
7	MISO_TRI_OPT	R/W	1: MISO stays low-Z even when SPI_SS=1. 0: MISO is tri-state when SPI_SS=1.	0B
6:0	SCRAMBLE_DATA	R/W	Whitening seed for data scramble. Must be set the same at both ends of radio link (Tx and Rx).	00H

9.16 Register 36

Table 22. Register 36 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[15:0]	R/W	LSB bits of sync word is sent first.	0000H

9.17 Register 37

Table 23. Register 37 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[31:16]	R/W	LSB bits of sync word is sent first.	0000H

9.18 Register 38

Table 24. Register 38 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[47:32]	R/W	LSB bits of sync word is sent first.	0000H

9.19 Register 39

Table 25. Register 39 information

Bit	Name	R/W	Description	default
15:0	SYNC_WORD[63:48]	R/W	LSB bits of sync word is sent first.	0000H

9.20 Register 40

Table 26. Register 40 information

Bit	Name	R/W	Description	default
15:11	FIFO_EMPTY_THRESHOLD	R/W		00100B
10:6	FIFO_FULL_THRESHOLD	R/W		00100B
5:0	SYNCWORD_THRESHOLD	R/W	The minimum allowable error bits of SYNCWORD, 07 means 6 bits，01 means 0 bit	07H

9.21 Register 41

Table 27. Register 41 information

Bit	Name	R/W	Description	default
15	CRC_ON	R/W	1: CRC on. 0: CRC off.	1B
14	SCRAMBLE_ON	R/W	Removes long patterns of continuous 0 or 1 in transmit data. Automatically restores original unscrambled data on receive. 1: scramble on. 0: scramble off.	0B
13	PACK_LENGTH_EN	R/W	1: HC24GB regards first byte of payload as packet length descriptor byte.	1B
12	FW_TERM_TX	R/W	1: When FIFO write point equals read point, HC24GB will terminate TX when FW handle packet length. 0: FW (MCU) handles length and terminates TX.	1B

Bit	Name	R/W	Description	default
11	AUTO_ACK	R/W	1: After receiving data, automatically send ACK/NACK. 0: After receive, do not send ACK or NACK; just go to IDLE.	1B
10	PKT_FIFO_POLARITY	R/W	1: PKT flag, FIFO flag Active low. 0: Active high	0B
9:8	(Reserved)	R/W	(Reserved)	00B
7:0	CRC_INITIAL_DATA	R/W	Initialization constant for CRC calculation.	00H

9.22 Register 42

Table 28. Register 42 information

Bit	Name	R/W	Description	default
15:10	SCAN_RSSI_CH_NO	R./W	Number of consecutive channels to scan for RSSI value. RSSI result of each channel is returned in FIFO registers.	00H
9:8	(Reserved)	R/W	(Reserved)	01B
7:0	Rx_ACK_TIME[7:0]	R/W	Wait RX_ack ID timer setting. 1 represents 1us	6BH

9.23 Register 43

Table 29. Register 43 information

Bit	Name	R/W	Description	default
15	SCAN_RSSI_EN	R./W	1: Start scan_RSSI process.	0B
14:8	SCAN_STRT_CH_OFFST[6:0]	R/W	Normally an RSSI scan would start at 2402 MHz (channel 0). This field introduces a starting offset. EXAMPLE: If offset= +10, Starting channel will be 2412 MHz (ch. 10).	01B
7:0	WAIT_RSSI_SCAN_TIM[7:0]	R/W	Set VCO & SYN setting time when scan different channel RSSI	6BH

9.24 Register 48 – Read only

Table 30. Register 48 information

Bit	Name	R/W	Description	default
15	CRC_ERROR	R	Received CRC error	
14	FEC23_ERROR	R	Indicate FEC23 error	
13:8	FRAMER_ST	R	Framer status	
7	SYNCWORD_RECV	R	1: syncword received, it is just available in receive status, After out receive status, always keep '0'.	
6	PKT_FLAG	R	PKT flag indication	
5	FIFO_FLAG	R	FIFO flag indication	
4:0	(Reserved)	R	(Reserved)	

9.25 Register 50

Table 31. Register 50 information

Bit	Name	R/W	Description	default
15:0	TXRX_FIFO_REG	R/W	For MCU read/write data between the FIFO. Reading this register removes data from FIFO; Writing to this register adds data to FIFO. Note: FW (MCU) access to FIFO is byte-by-byte.	00H

9.26 Register 52

Table 32. Register 51 information

Bit	Name	R/W	Description	default
15	CLR_W_PTR	W	1: clear TX FIFO point to 0 when write this bit to "1". It is not available in RX status.	0B
14	(Reserved)	W		
13:8	FIFO_WR_PTR	R	FIFO write pointer.	
7	CLR_R_PTR	W	1: clear RX FIFO point to 0 when write this bit to "1". It is not available in TX status.	0B
6	(Reserved)			
5:0	FIFO_RD_PTR	R	FIFO read pointer (number of bytes to be read by MCU).	

10 Recommended Register Values

The following register values are recommended for most typical applications. Some changes may be required depending on application.

Table 33. Recommended Register Values

Register number	Power-up reset value (hex)	Recommended value for many applications (hex)	Notes
0	6fef	6fef	
1	5681	5681	
2	6619	6617	
4	5447	9cc9	
5	f000	6637	
7	0030	0030	Use for setting RF frequency, and to start/stop Tx/Rx packets.
8	71af	6c90	
9	3000	1840	Sets Tx power level
10	7ffd	7ffd	Crystal osc. enabled.
11	4008	0008	RSSI enabled.
12	0000	0000	
13	4855	48bd	
22	c0ff	00ff	
23	8005	8005	Calibrate VCO before each and every Tx/Rx.
24	307b	0067	
25	1659	1659	
26	1833	19e0	
27	9100	1200	No crystal trim.
28	1800	1800	
29	00x0	read-only	Stores p/n, version information.
30	f413	read-only	Stores p/n, version information.
31	1002	read-only	Stores p/n, version information.
32	1806	1806	Packet data type: NRZ, no FEC, BRCLK=12 div. by 4= 3MHz
33	6307	3ff0	Configures packet sequencing.
34	030b	3000	Configures packet sequencing.
35	1300	0380	AutoAck max Tx retries = 3
36	0000	Choose unique sync words for each over-the-air network.	Similar to a MAC address.
37	0000		
38	0000		
39	0000		
40	2107	2107	Configure FIFO flag, sync threshold.
41	b800	b000	CRC on. SCRAMBLE off. 1st byte is packet length.
42	fd6b	fdb0	
43	000f	000f	Configure scan_rssi.

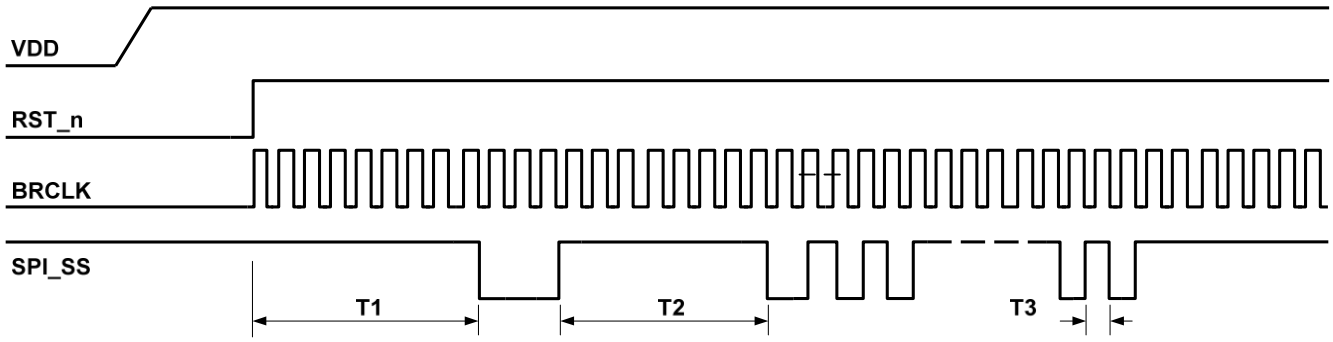
11 Usage Notes

The HC24GB Low-Cost RF Transceiver can be used to add wireless capability to many applications. The following notes are intended to answer common questions regarding the HC24GB.

11.1 Power On and Register Initialization Sequence

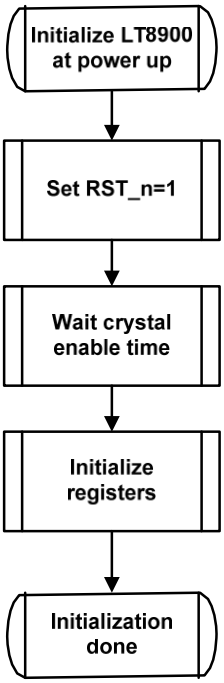
Figure below shows the timing diagram of power-on sequence after VDD is ready.

Figure 4. Power on and register programming sequence



1. After VDD power is ready, make sure to have valid reset on pin RST_n, which is active-low.
2. After RST_n =1, BRCLK will be running at 12MHz clock.
3. Wait T1 (1 to 5 ms) for crystal oscillator to stabilize, then MCU/application can perform register initialization.
4. After register initialization, HC24GB is ready to transmit or receive.

Figure 6. Initialization flowchart



11.2 Enter Sleep and Wake-Up

When MCU writes HC24GB register to enter sleep mode and pulls SPI_SS back to high, HC24GB will enter sleep state where the current consumption is extremely low. When SPI_SS is pulled low, HC24GB will automatically wake up from sleep state. MCU needs to keep SPI_SS low a certain time (the time required for RFIC crystal to be stabilized) before driving SPI_CLK and SPI data.

11.3 Packet Data Structure

Each over-the-air HC24GB packet is structured as follows:

- Preamble: 1~8 bytes, programmable.
- SYNC: 16/32/48/64 bits, programmable as device syncword.
- Trailer: 4~18 bits, programmable.
- Payload: TX/RX data. There are 4 data types:
  - Raw data
  - 8 bit / 10 bit line code
  - Manchester
  - Interleave with FEC option
- CRC: 16-bit CRC is optional.

11.4 FIFO Pointer Clear

For transmit, it is required to clear FIFO write pointer before application writes data to FIFO for transmit. This is accomplished by writing '0' to Register 52[15].
After receiving a packet, the read pointer will indicate how many bytes of receive data are waiting in FIFO buffer, waiting to be read by user MCU or application.

FIFO write pointer will automatically be cleared when receiver receives SYNC.
FIFO read pointer will automatically be cleared when receiver receives SYNC, or after transmitting SYNC in transmit mode.

11.5 Packet Payload Length

HC24GB provides two ways to handle TX/RX packet length. If Register 41[13]= 1, the HC24GB internal framer will detect packet length based on the value of the 1st payload byte. If Register 41[13]= 0, the 1st byte of the payload has no particular meaning, and packet length is determined by either TX FIFO running empty, or TX_EN bit cleared. See table below:

Table 34. Packet Payload Length

Register 41[13] PACK_LENGTH_EN	Register 41[12] FW_TERM_TX	
0 (MCU/application handles packet length)	0	Transmit stops only when Register 7 TX_EN= 0. See page 31 for details. Receive stops only when Register 7 RX_EN= 0. See page 33 for details.
	1	Transmit automatically stops whenever FIFO runs empty. Receive stops only when Register 7 RX_EN= 0. See page 29 for details.
1 (HC24GB framer handles packet length)	x (don't care)	1st byte of payload is regarded as packet length, 0 to 255 bytes. Transmit automatically stops when all 0 to 255 bytes are transmitted. See page 25 for details.

Detailed timing diagrams are shown below.
All timing diagrams show active-high for PKT and FIFO flags. Active-low is also available via Register 41[10] setting.

11.6 Framer handles packet length

Framer of HC24GB will handle packet length by setting Register 41[13]=1. The first byte of payload is regarded as packet length (this length byte is not counted in the packet length). Maximum allowed packet length is 255 bytes. Framer will handle Tx/Rx start and stop.

11.6.1 Transmit Timing

Tx timing diagram is shown below. After MCU writes Register 7[8]=1 and selects transmit channel (refer to Register 7 definition), the framer will automatically generate the packet using payload data from FIFO. MCU needs to fill in transmit data before framer sends trailer bits.
If packet length exceeds FIFO length, the MCU will need to write FIFO data multiple times. FIFO flag indicates whether FIFO is empty in transmit state or not.

Figure 5. Tx Timing Diagram when Register 41[13]= 1 (Framer Handles Packet Length).

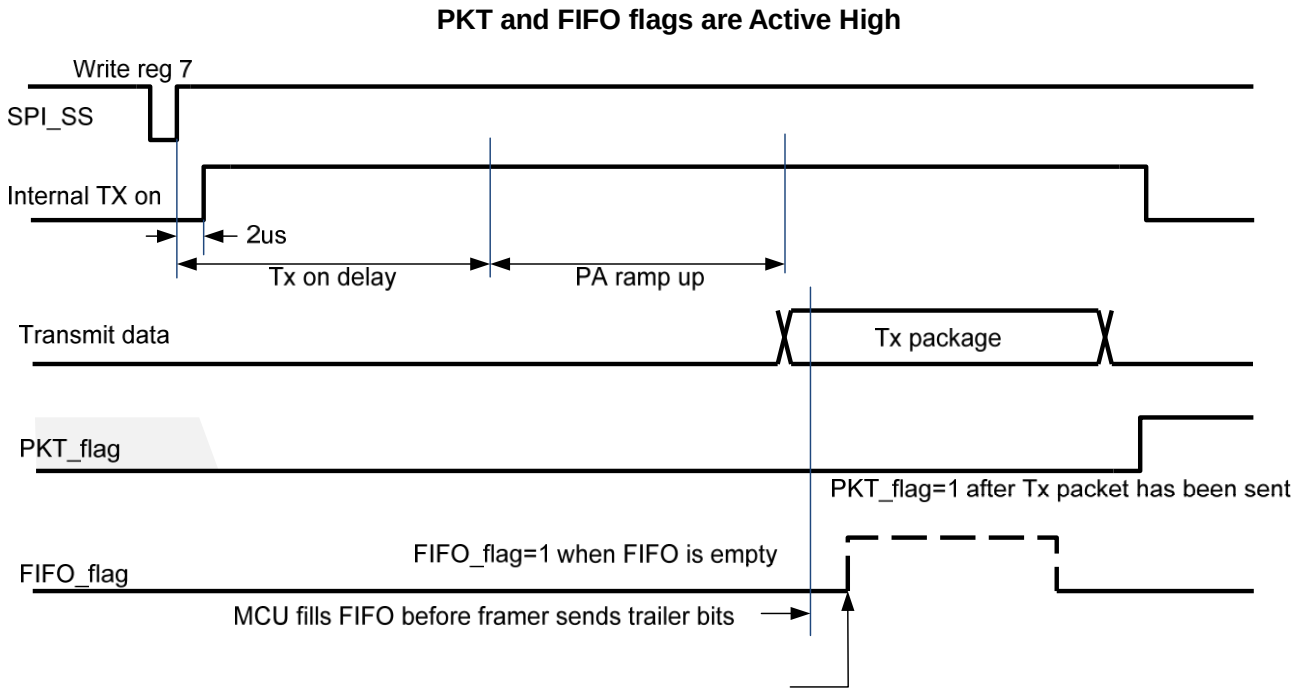
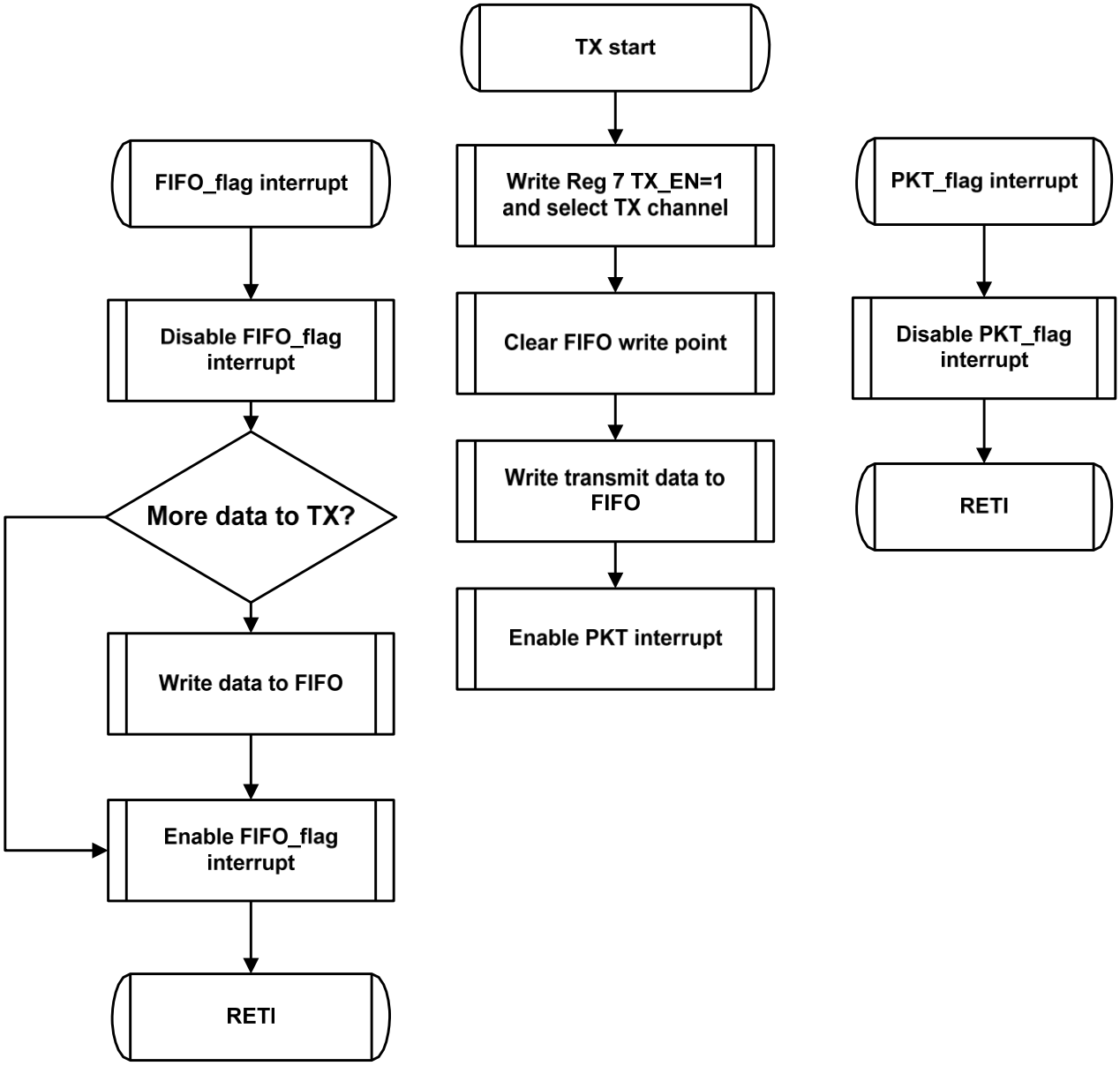


Figure 6. Example Tx packet flowchartwhere FIFO and PKT flags are interrupt signals to MCU.



11.7 Receive Timing

Rx timing diagram is shown in figure below. When MCU writes Register 7[7]= 1 and selects receiving channel, HC24GB framer will turn on the receiver and wait while attempting to detect a valid syncword.
If valid syncword is found, the HC24GB framer will process packet automatically. When received packet processing is complete, HC24GB framer will set state to IDLE.
If received packet length is longer than 63 bytes, FIFO flag will go active, which means MCU must read out data from FIFO.
A valid syncword will not always be found, due to weak signal, multipath signal cancellation, devices out of range, etc. To accommodate such a condition and prevent lockup, the MCU/application should incorporate a receive timeout timer. In most applications, receive packets are expected to arrive within a defined time 'window'. If the packet does not arrive, the system can use either timer polling or timer-based interrupt to take corrective or alternative action.

Figure 7. Rx Timing Diagram when Register 41[13]=1 (Framer Handles Packet Length).

PKT and FIFO flags are Active High

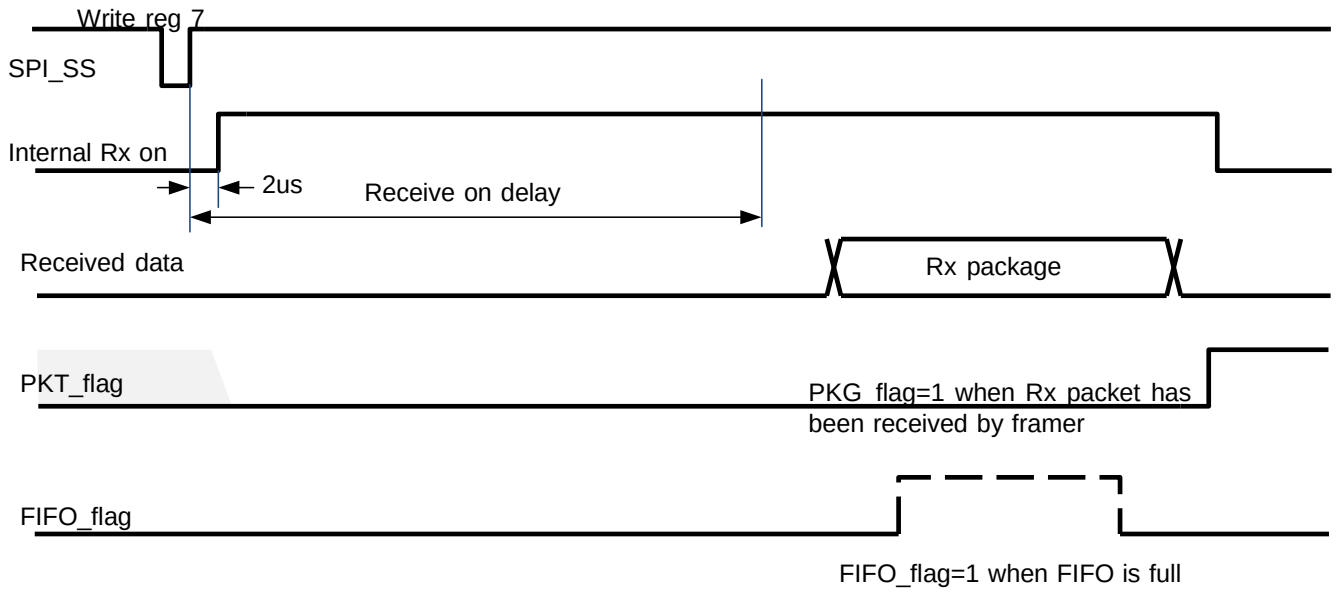
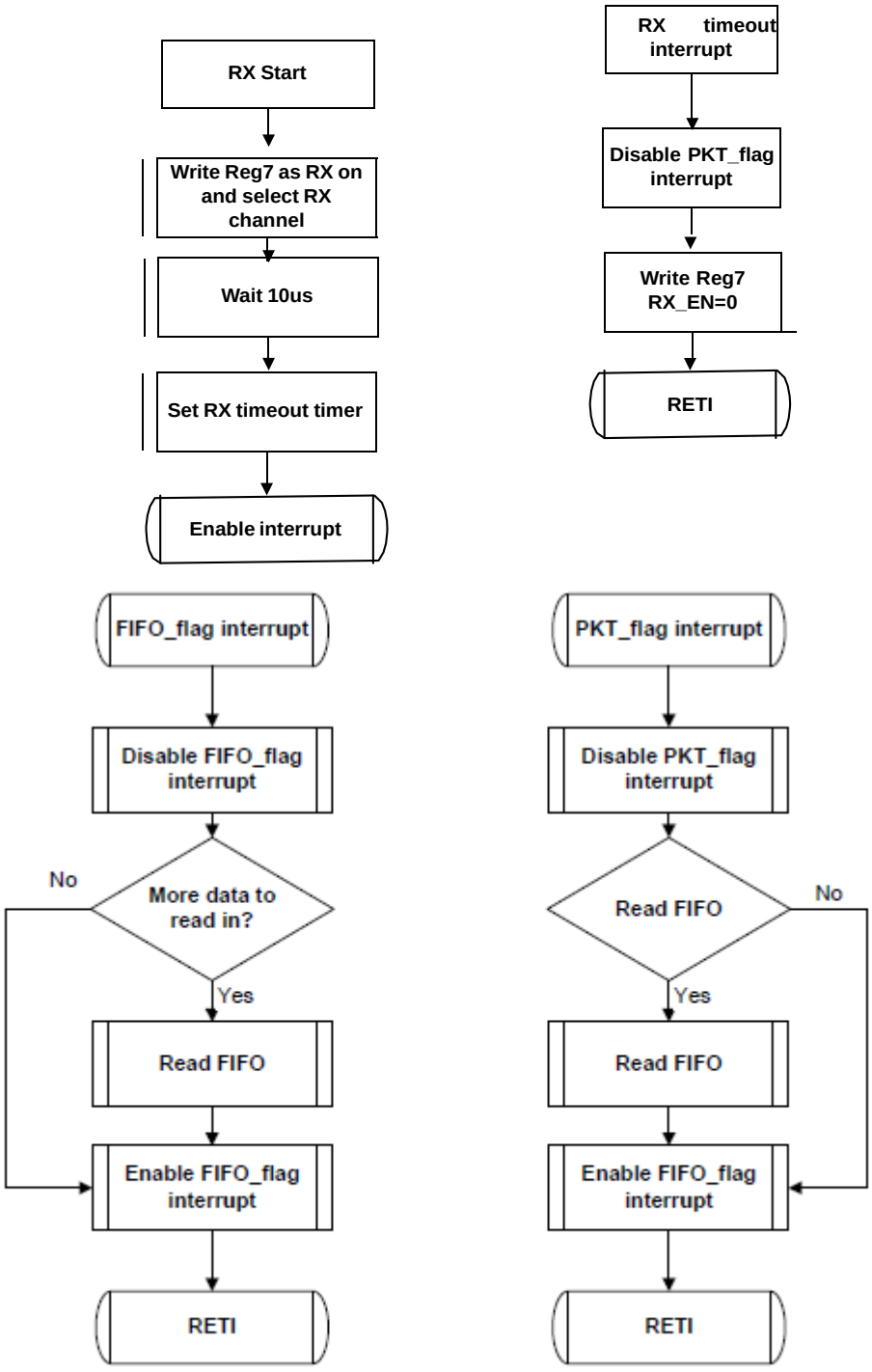


Figure 8. Example Rx packet flowchart where FIFO and PKT flag signals interrupt MCU.



11.8 MCU/Application handles packet length

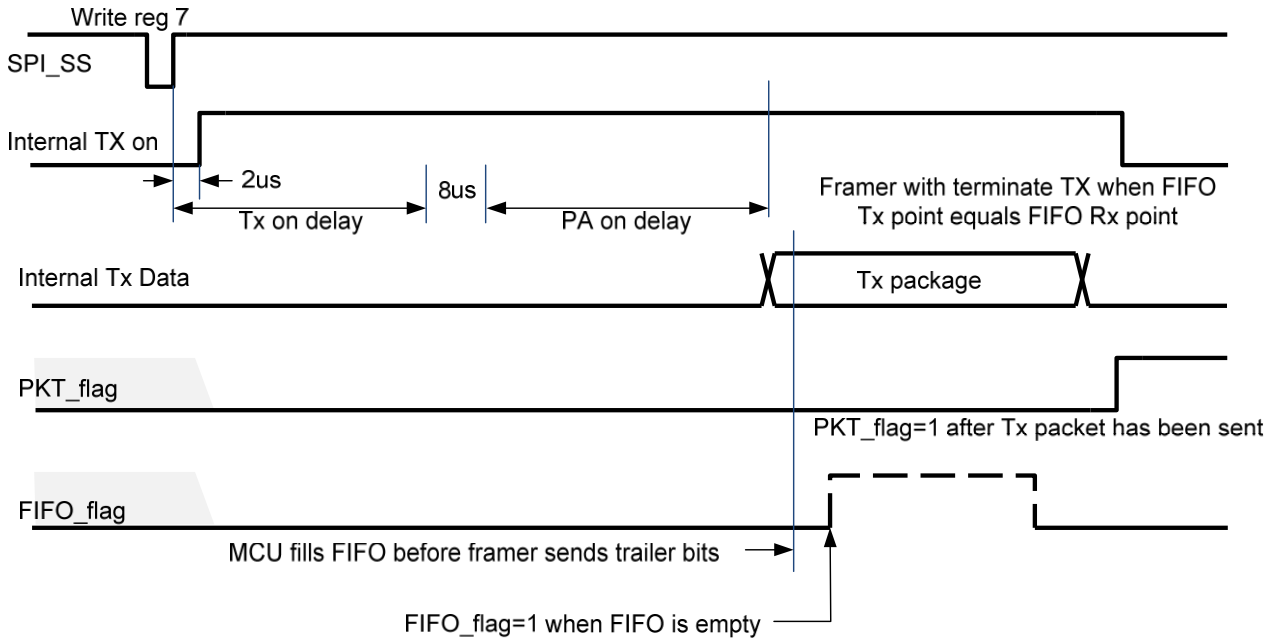
When Register 41[13]= 0, the 1st byte of the payload data has no special significance. Instead, packet length depends on Register 41[12].

11.8.1 FW_TERM_TX= 1

If Register 41[12] = 1, the HC24GB framer will continue to compare FIFO write point and FIFO read point during packet transmission. If MCU/application stops writing data to FIFO, the framer eventually detects that there is no data to send (FIFO empty), and HC24GB will exit cease transmission automatically. The timing diagram is shown in Figure below.

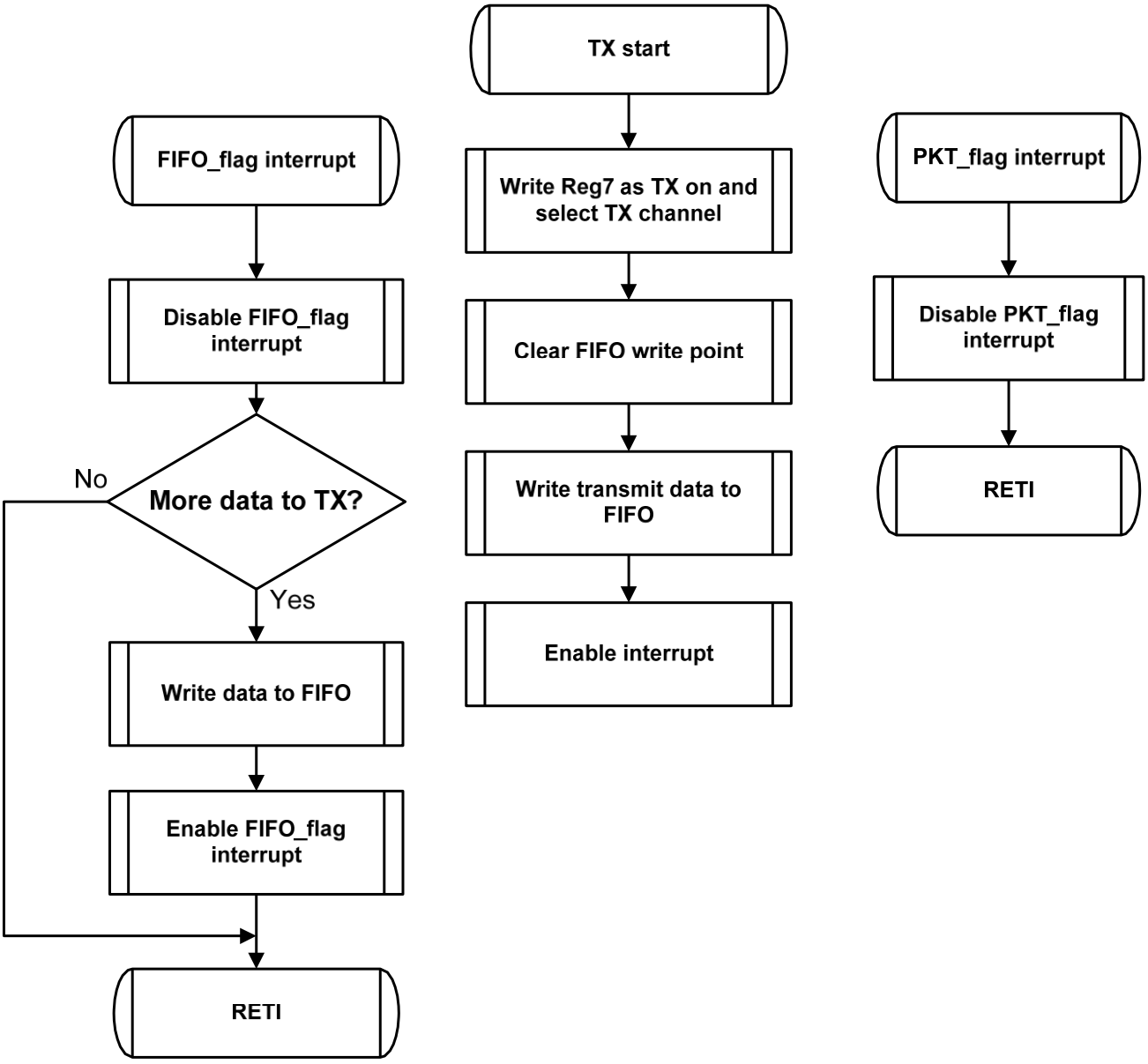
Figure 9. Tx timing when Register 41[13:12]= 'b01.

PKT and FIFO flags are set as active high.



Note: When Register 41[13] = 0 (MCU/application handles packet length), never let FIFO underflow or over flow. FIFO full/empty thresholds can be controlled via Register 40 FIFO_EMPTY_THRESHOLD and FIFO_FULL_THRESHOLD settings. The best value will depend on SPI speed, and speed at which MCU/application can stream the data into FIFO.

Figure 10. Example transmit flowcharts for Register 41[13:12]= 'b01 using interrupts for PKT and FIFO flags.

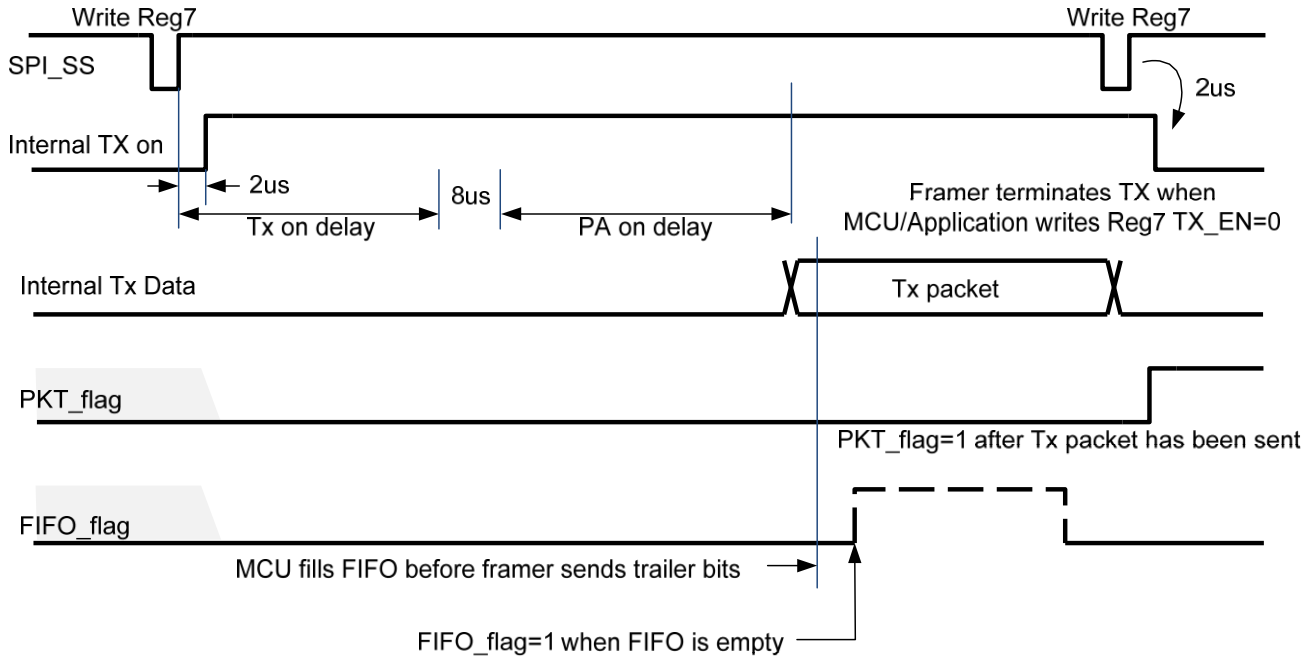


11.8.2 FW_TERM_TX= 0 (Transmit)

When Register 41[13:12] = ‘b00, the HC24GB framer does not stop packet transmission until MCU/application writes Register 7[8] TX_EN bit = 0. Packet transmission continues even if FIFO is empty. The timing diagram is shown in Figure below.

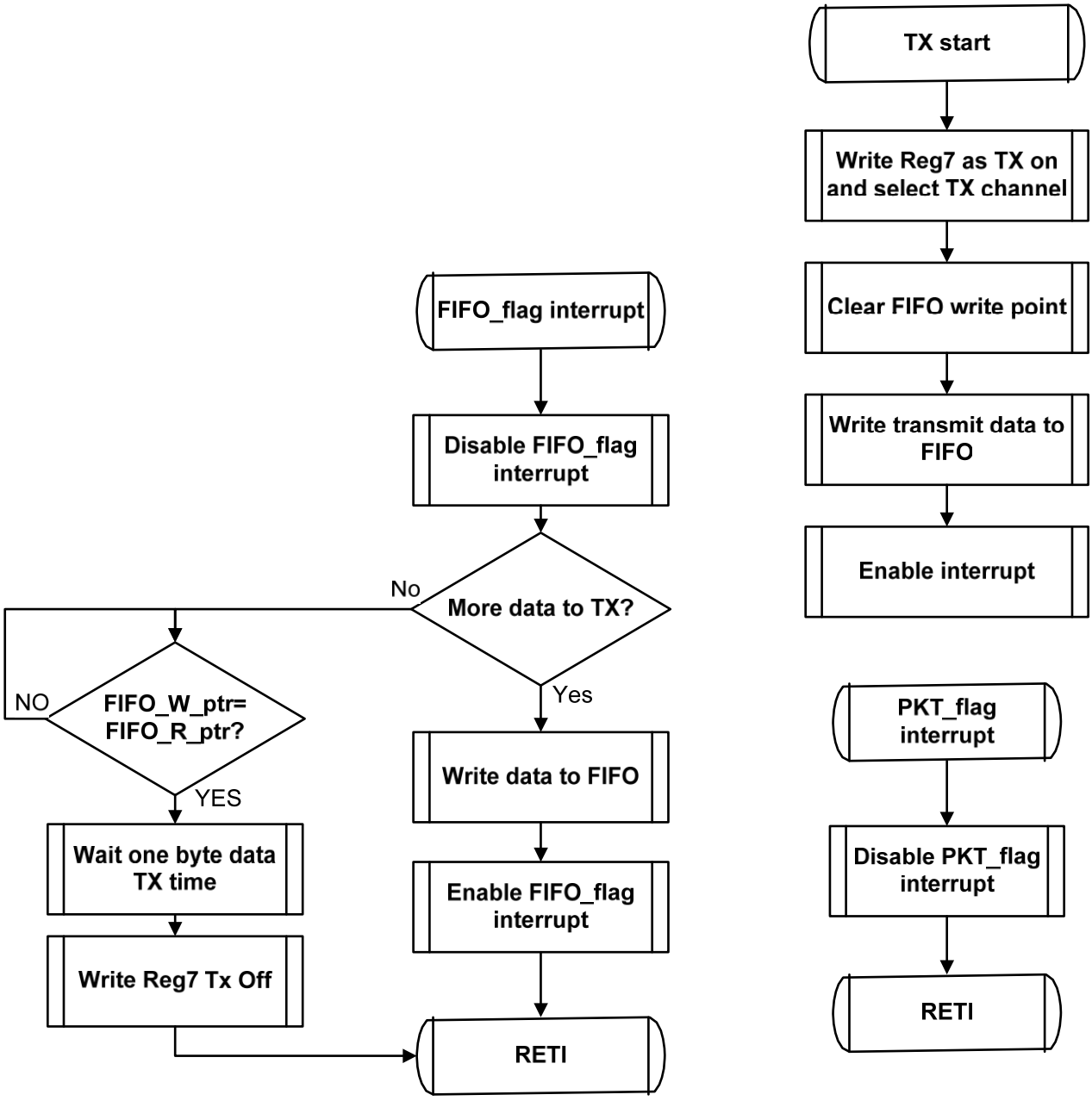
Figure 11. TX timing diagram when Register 41[13:12] = ‘b00.

PKT and FIFO flags are shown high active.



Note: When Register 41[13] = 0 (MCU/application handles packet length), never let FIFO underflow or over flow. FIFO full/empty thresholds can be controlled via Register 40 FIFO_EMPTY_THRESHOLD and FIFO_FULL_THRESHOLD settings. The best value will depend on SPI speed, and speed at which MCU/application can stream the data into FIFO.

Figure 12. Example Transmit flowcharts for Register 41[13:12]= 'b00 using interrupts for PKT and FIFO flags.



11.8.3 FW_TERM_TX= 0 (Receive)

When Register 41[13] =0, packet reception starts when MCU/application writes Register 7[7] RX_EN = 1. At this time, the framer will automatically turn on the receiver to the frequency/channel specified in register 7. After waiting for the internal synthesizer and receiver delays to transpire, the framer circuitry of the HC24GB will begin searching the incoming signal for a syncword. When detected, it will set PKT flag active, then start to fill FIFO with receive data bytes. The PKT flag will remain active until MCU/application reads out the first byte of data from FIFO register. After MCU/application reads the first byte of receive data, PKT flag goes inactive until next Tx/Rx period.
With Register 41[13:12] = ‘b00 or ‘b01, the HC24GB framer will always need the MCU/application to write Register 7[7] to 0 to stop Rx state.
Rx timing diagram is shown in Figure below.

Figure 13. RX timing diagram when Register 41[13:12] = ‘b00 or ‘b01.

PKT_flag and FIFO_flag are active high.

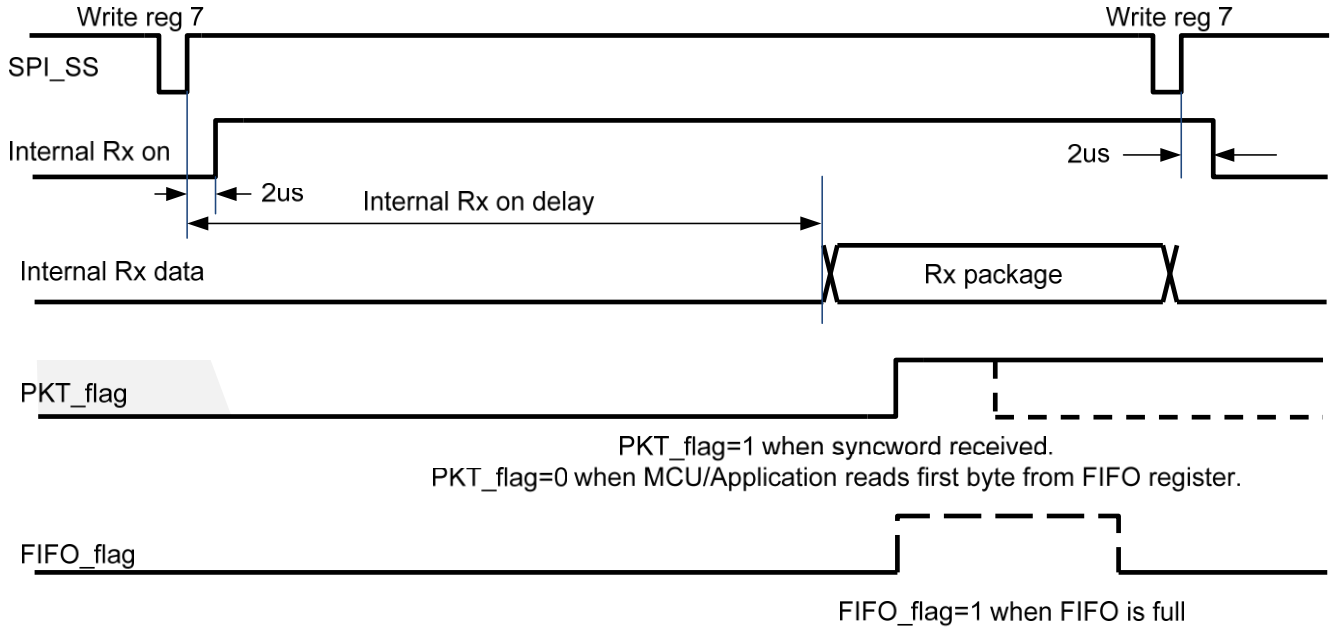
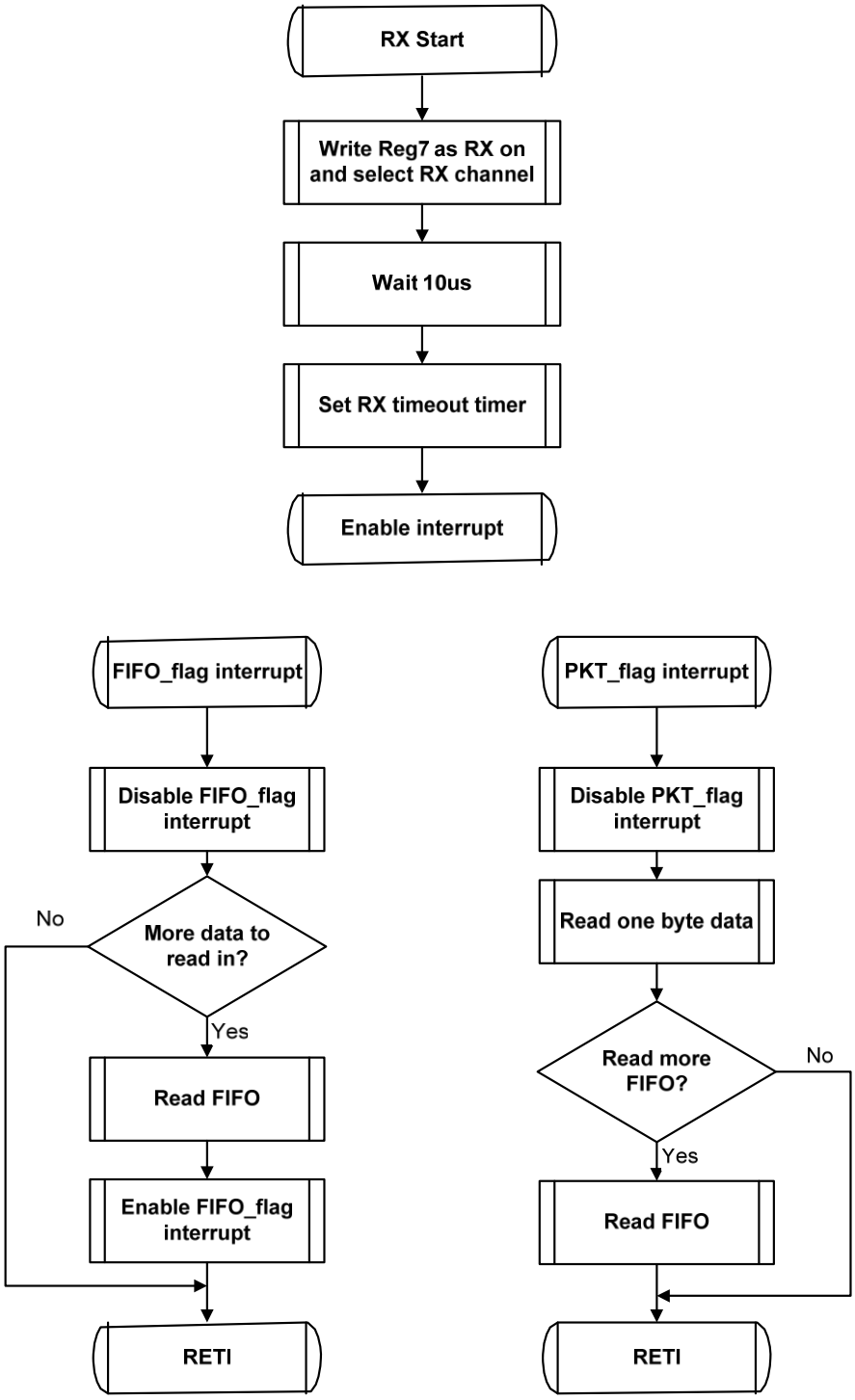


Figure 14. Example Receive flowcharts for Register 41[13:12]= 'b00 or 'b01 using interrupts for PKT and FIFO flags.



11.9 Crystal Oscillator

The HC24GB supports quartz crystal, or external clock input.

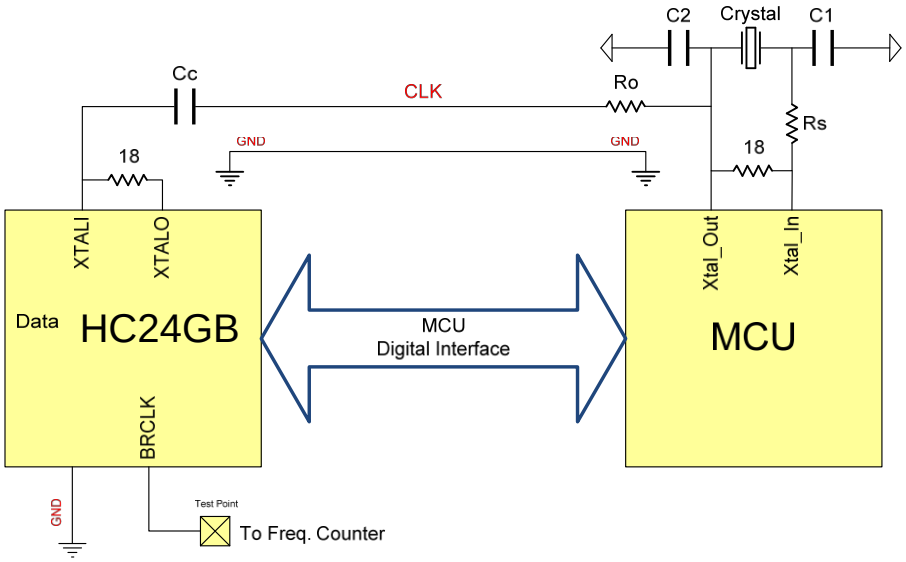
11.9.1 Quartz crystal application

Series resistor R2 limits power to the crystal, and contributes to the phase shift necessary for oscillation. Crystal loading capacitors C7 and C8 largely determine the load seen by the crystal, which should match the crystal vendor's specification. These capacitor values can be trimmed, to fine-tune the frequency of oscillation. Self- bias resistor R1, from buffer output to input, serves to self-bias the on-chip buffer to the center of the linear region for maximum gain.

11.9.2 External clock application

Self-bias resistor R1 should still be used, but the external clock may be coupled to the XTALI pin via a series DC blocking capacitor. See circuit below.
Output resistor R0 is used to sample a small amount of power from an existing oscillator or clock circuit. The best value of R0 may need to be determined experimentally, but around 3k Ohms is a good starting point. In the extreme case of R0 being much too large, the RFIC will fail to initialize to the IDLE state properly.
Regarding PCB layout: The CLK trace should be kept short and direct. The trace should be relatively narrow (high impedance), and must route away from other traces on the PCB that may inject or couple noise onto the CLK trace. The HC24GB will receive the clock signal relative to ground; therefore, the ground between chips should be a good low-noise, low-inductance ground. Ideally, this GND return should be a single ground plane on the PCB layout.

Figure 15. External Clock Application



Additional Notes:

1. ***Clock duty cycle should be 50%. If not 50%, some additional drive voltage may be required (i.e. reduce R0).***
2. ***If received Bit Error Rate (BER) is high, it can be caused by insufficient clock drive to the RFIC (i.e. reduce R0).***
3. ***Another cause for high BER is phase noise on the clock signal. Try putting 0.1 and 2.2 uF ceramic bypass capacitors across the baseband chip VDD/VSS pins that power the oscillator.***

11.9.3 Minimum Pin Count

When a low cost MCU drives the HC24GB, MCU pin count must be minimized. Consider the following:

- FIFO: only needed when Tx or Rx packet length is greater than around 63 bytes, up to infinity. For short packets (< 63 bytes), FIFO is not needed.
- PKT: gives a hardware indication of a packet received. If the user is willing to poll register 48 for this information, then this pin is not needed.
- SPI lines: All 4 of these lines are needed.
- RST_n: This line is sometimes connected through an RC filter to the VDD_IN, which makes the chip self-reset when power is applied, thus eliminating an MCU pin.

11.9.4CKPHA

On the HC24GB die, there is a CKPHA pad. When HC24GB is purchased in QFN package, this pad will normally be connected by bond wire to a source of logic '1'. This is to save a pin, thus keeping packaged part cost low.
The alternate configuration, CKPHA= 0, is available by special order.
Customers ordering bare unpackaged die will be able to bond CKPHA however desired.

11.9.5 Antenna Type and Location

Probably the greatest single factor affecting RF performance for the HC24GB or any other over-the-air RF device is the antenna – not just type, but also placement and orientation. Antenna gain is normally measured with respect to isotropic, that is, an ideal radiator that sends/receives power equally from/to any direction. This ideal antenna would be described as 0 dBi, or zero dB's above/below isotropic. Unfortunately, they don't really exist in practice. A simple dipole with a theoretical gain of +2 dBi is usually a good choice, but the designer should exercise care when placing the antenna, since dipole antennas have a radiation pattern described as a donut, whereby the null can be very deep.
For most wireless applications, the printed full-wave loop antenna shown on the schematic should perform well, provided that the antenna is placed in the clear, away from other circuitry and wires, hands, etc. In particular, the antenna must be kept away from human tissue, particularly sensitive spots like the heart, brain, and eyes. Violating this design principle
will not only make the end product perform poorly and possibly become a long term danger to the user, but it will likely not receive FCC or other regulatory agency approval. For best operation, design the product so the main antenna radiation is away from the body, or at least not proximity loaded by the human body, or dielectric objects within the product.
Also, be sure to keep the antenna away from clock lines and digital bus signals; otherwise, harmonics of the clock frequency will jam certain receive frequencies. It's best to just keep the antenna away from all wires and metal objects!

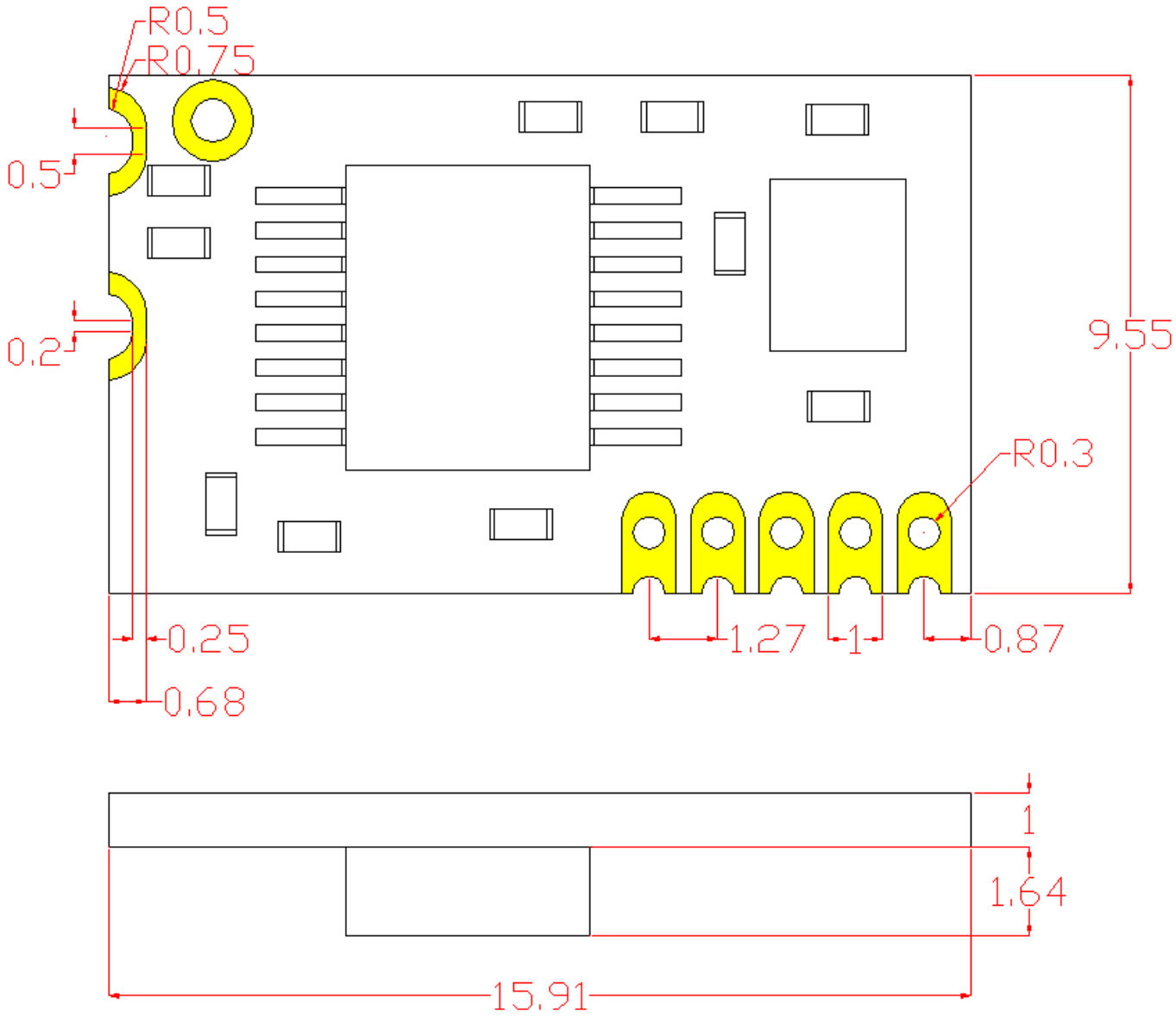
11.10 PCB Layout

PCB layout is not too critical, but here are some helpful hints:

1. RF path: Since the HC24GB utilizes 2-conductor balanced transmission line at the RF port, ground plane is not necessary along the balanced line length. Be sure to keep each of the two conductors equal length.
2. Clock traces: It is best to keep the clock traces simple and direct. The self-bias resistor should be close to the XTALI and XTALO pins. The oscillation loop, consisting of the series resistor and crystal, should be a simple, small loop. The crystal loading capacitors should be near the crystal. The ground connection to these capacitors must be to a good, clean, quiet ground. This keeps noise from becoming injected into the oscillator. This is a good reason to have one ground plane for the entire RF section.
3. Power distribution and decoupling: Capacitors should be located near the VDD pins, as shown in the schematic.
4. Antenna Placement: If using an antenna manufactured by a particular company, be sure to follow the manufacturer's recommendation regarding layout.
5. Digital Interface: In order to provide a good ground return for the digital lines, it is a good idea to provide at least 2 pins for ground, not just one. Good grounding between RF and MCU can help reduce noise 'seen' at the antenna, thus improving performance.

12 Module Package Outline Drawing

Unit: mm



13 IR Reflow Standard

Follow : IPC/JEDEC J-STD-020 B

Condition : Average ramp-up rate (183ºC to peak): 3 ºC/sec. max.

Preheat: 100~150ºC 60~120sec

Temperature maintained above 183ºC: 60~150 seconds

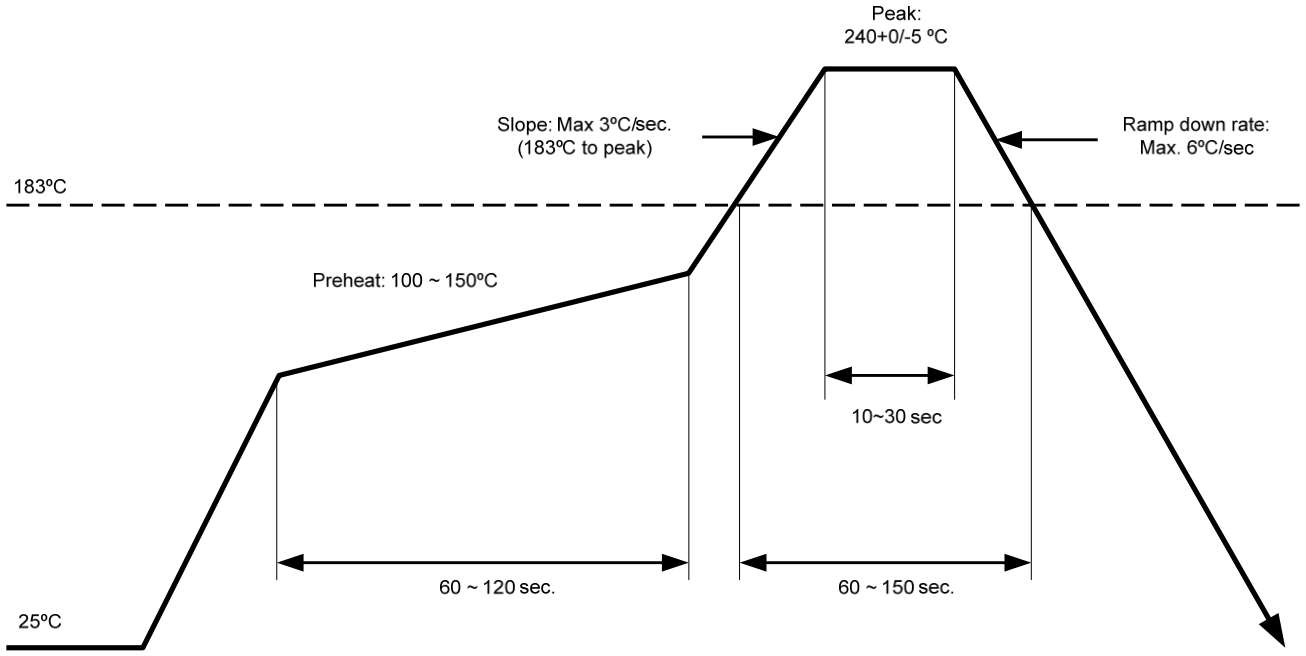
Time within 5ºC of actual peak temperature: 10 ~ 30 sec.

Peak temperature: 240+0/-5 ºC

Ramp-down rate: 6 ºC/sec. max.

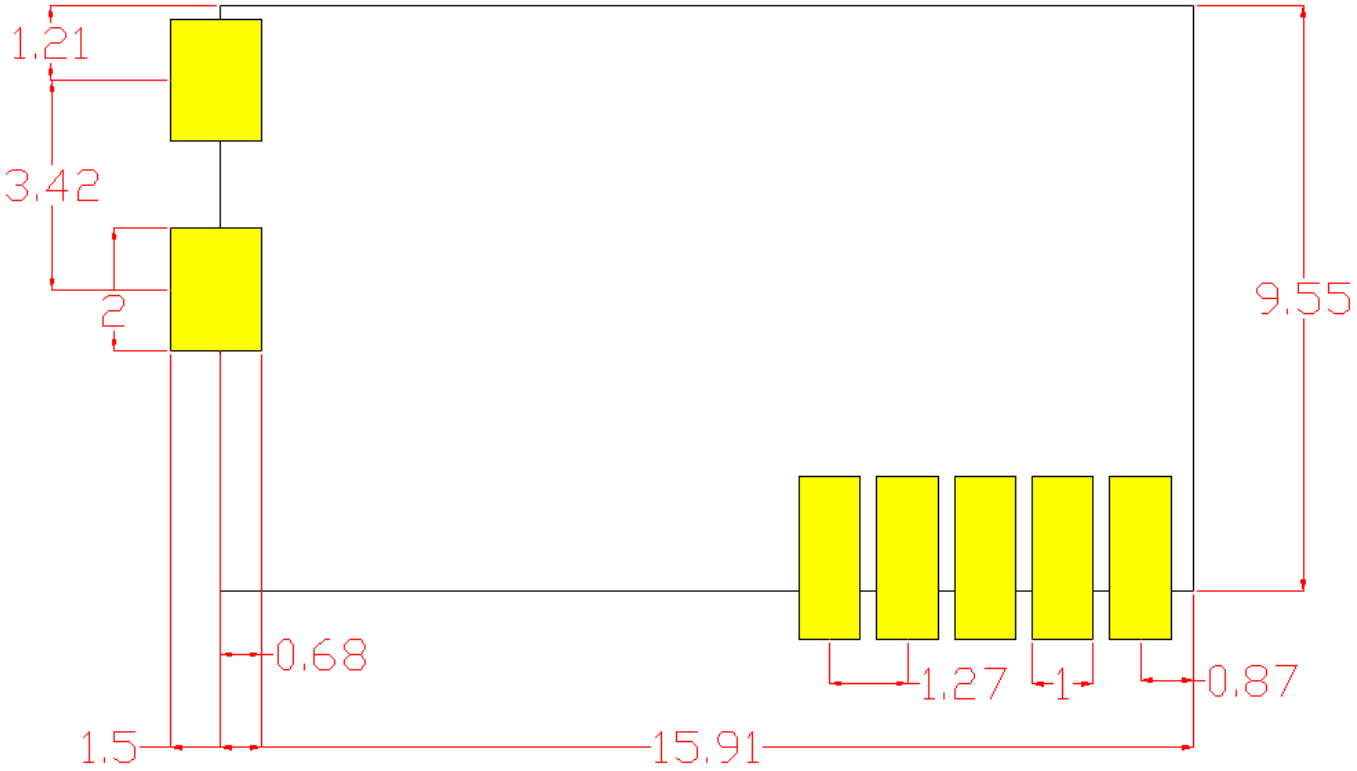
Time 25ºC to peak temperature: 6 minutes max. Cycle interval: 5 minutes

Figure 16. IR Reflow Diagram



14 Recommended PCB Land Pattern

Unit: mm



15 Tray Packaging

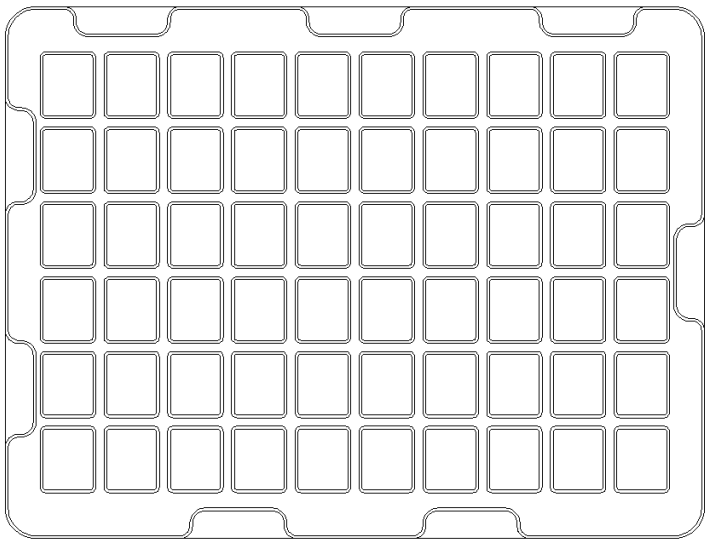
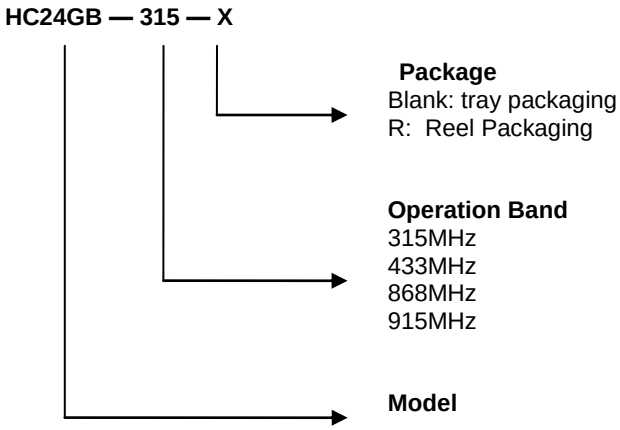


Figure 17.Package Outline Drawing

Note:

tray packaging, 60pcs/tray.

16 Ordering Information:



17 Module Revisions:

Table 35 Revision History

Revisions	Date	Updated History
Rev 1.0	Mar 2014	The first release

18 Contact us:

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