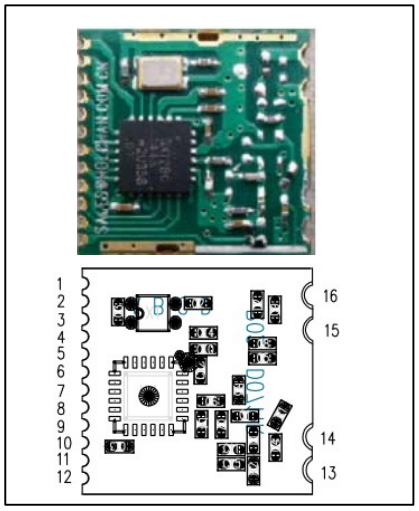
HC1239
FSK/OOK Receiver Module

1.General:

The HC1239 is a highly integrated RF receiver capable of operation over a wide frequency range, including the 433,868 and 915 MHz license-free ISM (Industry Scientific and Medical) frequency bands. Its highly integrated architecture allows for a minimum of external components whilst maintaining maximum design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The HC1239 offers the unique advantage of programmable narrow-band and wide-band communication modes without the need to modify external components. The HC1239 is optimized for low power consumption while offering high sensitivity and channelized operation. TrueRF™ technology enables a low-cost external component count (elimination of the SAW filter) whilst still satisfying ETSI and FCC regulations.



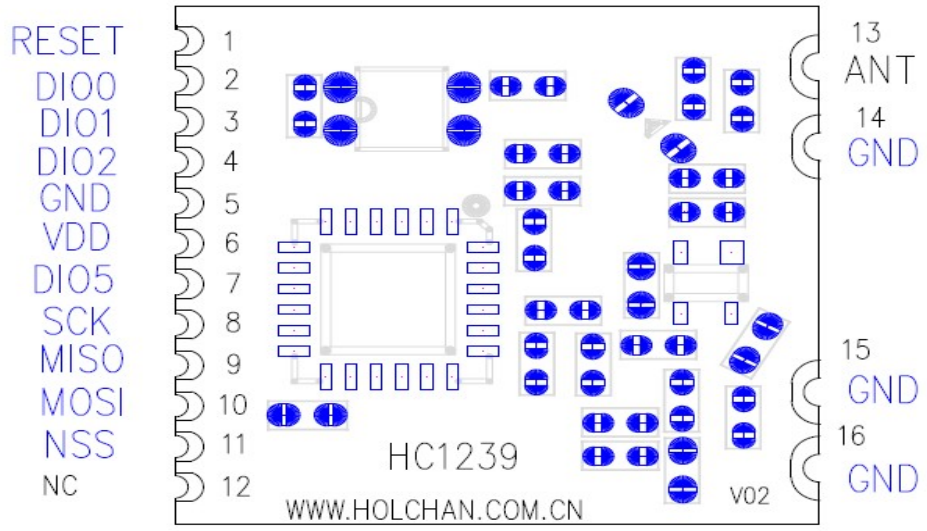
2.APPLICATIONS:

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless M-BUS

3.FEATURES:

- High Sensitivity: down to -120 dBm at 1.2 kbps
- High Selectivity: 16-tap FIR Channel Filter
- Bullet-proof front end: IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB Blocking Immunity, no Image Frequency response
- Low current: Rx = 16 mA, 100nA register retention
- Constant RF performance over voltage range of chip
- FSK Bit rates up to 300 kb/s
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK demodulation
- Built-in Bit Synchronizer performing Clock Recovery
- Incoming Sync Word Recognition
- 115 dB+ Dynamic Range RSSI
- Automatic RF Sense with ultra-fast AFC
- Packet engine with CRC, AES-128 encryption and 66- byte FIFO
- Built-in temperature sensor and Low Battery indicator

4.PIN DESCRIPTION



PIN No.	Name	I/O/P	Description
1	RESET	I/O	Module Hardware Reset, low pulse active
2	DIO0	I/O	Module Digital I/O 0, can define by module Register.
3	DIO1	I/O	Module Digital I/O 1, can define by module Register.
4	DIO2	I/O	Module Digital I/O 2, can define by module Register.
5	GND	P	Module Power supply Negative, Groud
6	VDD	P	Module Power supply Positive
7	DIO5	I/O	Module Digital I/O 5,can define by module Register
8	SCK	I	SPI Module clock input
9	MISO	O	SPI Master input and Slave output
10	MOSI	I	SPI Master output and Slave input
11	NSS	I	SPI Module Select control
12	NC		Not connect
13	ANT	O	Module Antenna terminal, Default terminal
14-16	GND	P	Module power supply Negative,Ground

P: is power supply

5.Electrical Characteristics

5.1.Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	° C
Tj	Junction temperature	-	+125	° C
Pmr	RF Input Level	-	+6	dBm

5.2 Operating Range

Table Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.6	V
Top	Operational temperature range	-40	+85	°C
Clop	Load capacitance on digital ports	-	25	pF
ML	RF Input Level	-	0	dBm

5.3 Power Consumption

Table Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.1	1	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	uA
IDDST	Supply current in standby mode	Crystal oscillator enabled	-	1.25	1.5	mA
IDDFS	Supply current in synthesizer mode		-	9	-	mA
IDDR	Supply current in receive mode		-	16	-	mA

5.4Frequency Synthesis

Table Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer Frequency Range	Programmable	290 424 862	- - -	340 510 1020	MHz MHz MHz
FXOSC	Crystal oscillator frequency	See section 7.1	-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time		-	250	500	us
TS_FS	Frequency synthesizer wake-up time to PllLock signal	From Standby mode	-	80	150	us
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 80 80 80	- - - - - - -	us us us us us us us
FSTEP	Frequency synthesizer step	FSTEP = FXOSC/2^{19}	-	61.0	-	Hz
FRC	RC Oscillator frequency	After calibration	-	62.5	-	kHz
BRF	Bit rate, FSK	Programmable	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps

5.5 Receiver

All receiver tests are performed with *RxBw* = 10 kHz (Single Side Bandwidth) ,receiving a PN15 sequence with a BER of 0.1% (Bit Synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level.

Table Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s	- - -	-118 -114 -105	- - -	dBm dBm dBm
		FDA = 5 kHz, BR = 1.2 kb/s*	-	-120	-	dBm
RFS_O	OOK sensitivity, highest LNA gain	BR = 4.8 kb/s	-	-112	-109	dBm
CCR	Co-Channel Rejection		-13	-10	-	dB
ACR	Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	- 37	42 42	- -	dB dB

BI	Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	66 71 79	- - -	dB dB dB
	Blocking Immunity Wanted signal at sensitivity +16dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	62 65 73	- - -	dB dB dB
AMR	AM Rejection , AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	66 71 79	- - -	dB dB dB
IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	- -	+75 +35	- -	dBm dBm
IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	- -23	+20 -18	- -	dBm dBm
BW_SSB	Single Side channel filter BW	Programmable	2.6	-	500	kHz
IMR_OOK	Image rejection in OOK mode	Wanted signal level = -106 dBm	27	30	-	dB
TS_RE	Receiver wake-up time, from PLL locked state to *RxReady*	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	- -	1.7 96	- -	ms us
TS_RE_AGC	Receiver wake-up time, from PLL locked state, AGC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	-	3.0 163		ms us
TS_RE_AGC &AFC	Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s		4.8 265		ms us
TS_FEI	FEI sampling time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_AFC	AFC Response Time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_RSSI	RSSI Response Time	Receiver is ready	-	$2.T_{bit}$	-	-
DR_RSSI	RSSI Dynamic Range	AGC enabled Min Max	- -	-115 0	- -	dBm dBm

5.6 Digital Specification

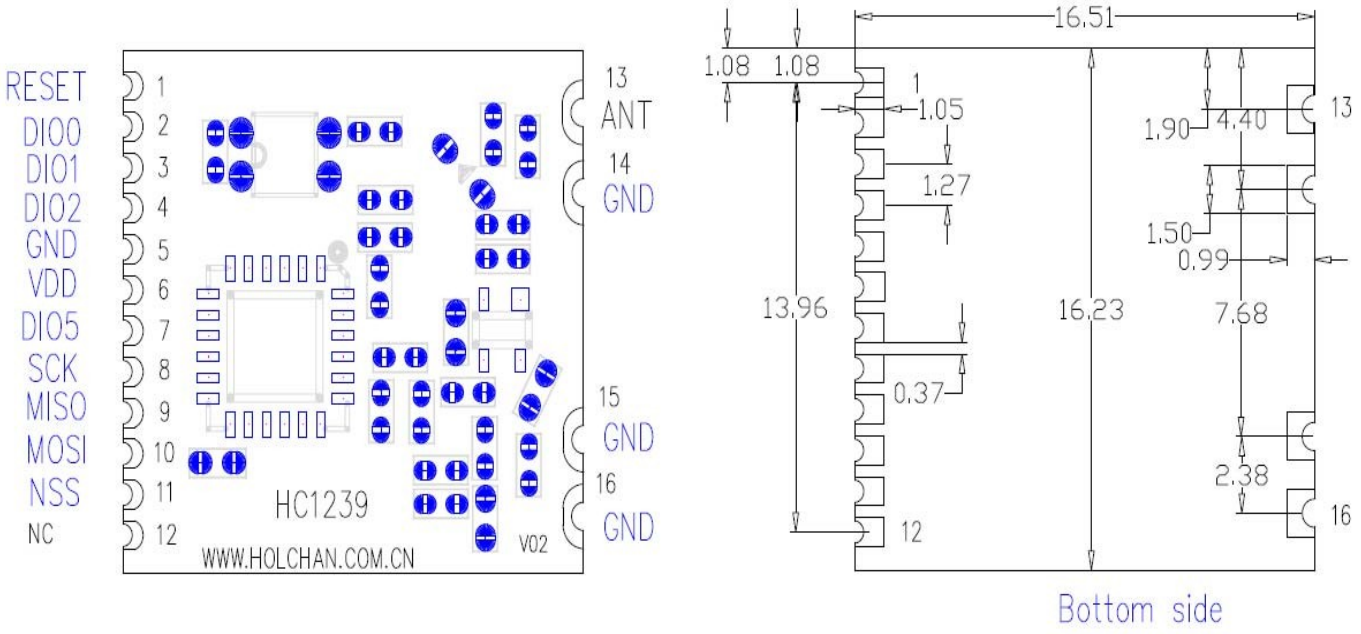
Conditions: Temp = 25°C, VDD = 3.3V, FXOSC = 32 MHz, unless otherwise specified.

Table Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VDD
V_{IL}	Digital input level low		-	-	0.2	VDD
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK frequency		-	-	10	MHz
t_{ch}	SCK high time		50	-	-	ns
t_{cl}	SCK low time		50	-	-	ns
t_{rise}	SCK rise time		-	5	-	ns
t_{fall}	SCK fall time		-	5	-	ns
t_{setup}	MOSI setup time	from MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	from SCK rising edge to MOSI change	60	-	-	ns
t_{nsetup}	NSS setup time	from NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	from SCK falling edge to NSS rising edge, normal mode	100	-	-	ns
t_{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

6. Module Package Outline Drawing

Unit: mm



7. Module Revisions

Revisions	Date	Updated History
Rev1.0	March 2014	The first final release
Rev1.1	June 2014	Update Module parameter for 868MHZ. 915MHZ

8. Importance Notice

The HC1239 datasheet will be changed by LJ ELECTRONICS TECHNOLOGY LIMITED according to the module design.

9.Contact us

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